Conducted emission simulation and measurement of interleaved DC-DC converters

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Abstract—Switching-Mode Power Supplies (SMPS) are often used to power on-board satellite payloads due to their good conversion efficiency. However, they emit radiated and conducted noise, which can disturb the operation of other payloads. The current ripple sum of the power supplies will appear on the power bus. There are many methods to reduce this summarized noise, one of them is to interleave the on-switching times of the converters. This ripple cancellation method can decrease the noise component on the switching frequency and on its upper harmonics. In this article we are going to demonstrate the effects of the distributed interleaving with a measurement platform consisting of two Pulse Width Modulation (PWM) controlled Buck controllers.

Index Terms—switching-mode power supply, interleaving, conducted emission measurement, satellite power system

Fig. 1 LTspice Simulation block diagram

I. INTRODUCTION

ON-board a satellite there are various payloads, which require different voltage levels to function. Switching-mode power supplies are typically used to convert the voltage of the power bus to the adequate level. In a satellite power system the inputs of the converters are parallel connected and because of this their input current ripples will be summarized on the bus. There are different regulations to limit the noise emission of the converters (e.g. European Cooperation for Space Standardization (ECSS) standard). Most of the time differential and common mode filters are used for noise mitigation. However, these filters often contain bulky components requiring a lot of space. In case of constant-frequency controlled power supplies the switching periods can be synchronized by an external clock. The phases of converter oscillator signals can be set to different values. With this phase division the on-switching times can be interleaved. In the case of two interleaved converters their input current ripples will be 180 degree out of phase, so they will cancel each other on the power bus [1]-[4]. The frequency of the summarized input current will be twice of the original, which can be filtered out with a smaller capacitor [3]. In the following chapters we will present the effects of the distributed interleaving with a setup consisting of two Buck converters. The setup was simulated in LTspice XVII (v.17.0.34.0) [5] simulation environment and later it was built and measurements were conducted.
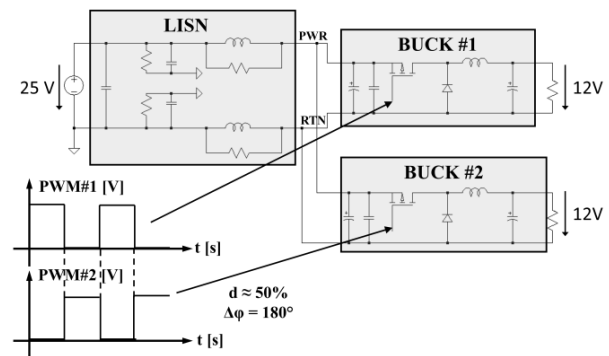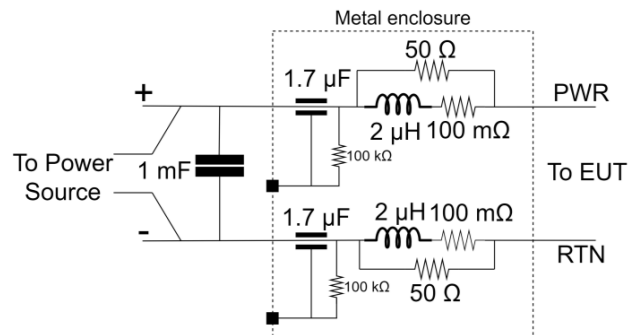

Fig. 2 LISN block diagram [7]

II. INTERLEAVING METHOD SIMULATION

The block diagram of the simulation can be seen in Fig 1. The task of the Line Impedance Stabilization Network (LISN) is to simulate the impedance of the satellite power bus and to isolate the Buck converters from external conducted disturbances [6], [7]. The LISN was made according to the Electromagnetic Compatibility (EMC) ECSS standard and its block diagram can be seen in Fig 2 [7]. The 1 mF capacitance represents the bus capacitance. The 2 µH coils and the 100 mΩ resistances simulate the series inductance and resistance of the satellite harness. At higher frequencies the two 1.7 µF capacitances will shunt the 100 kΩ resistors, and the two 50 Ω resistors will be in series, making their net resistance 100 Ω, which is the typical characteristic impedance of the satellite harness.

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In the simulations the converter Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) were driven by two 50 kHz square signals, the duty cycle of both signals were ~ 50 %. In Fig 1. we can see that the phase delay between the signals is 180°. In case of a signal with 50 kHz frequency (20 µs time period) this phase delay translates to 10 µs time delay. The input bus voltage of the converters was 25 V, their output voltage was 12 V and their max output power was 48 W. In the simulation the output current of the converters were set to the same value.

To characterize the behavior of the system, the input currents of the converters and their summarized current were observed in time domain and then were converted into spectrum with Fast-Fourier Transform (FFT) algorithm [8]. In Fig 3 and 4 we can see the simulation results. On top there is the summarized input current ripple of the converters and below is the current spectrum. From the figures we can see that the noise component on the 50 kHz switching frequency is completely diminished and the signal frequency is 100 kHz, the double of the original [9]. The main components of the spectrum are the upper harmonics of this doubled frequency. In this simulation the value of the choke inductances and the driving signal duty cycles were completely identical. These are ideal conditions because the components would have a finite tolerance. Also, in case of individually controlled converters the duty cycles would not exactly match. If we repeat the same simulation but with 1% choke inductance value tolerance and with slightly unmatched converter duty cycles, then we will get the results in Fig 5 and 6 [1].
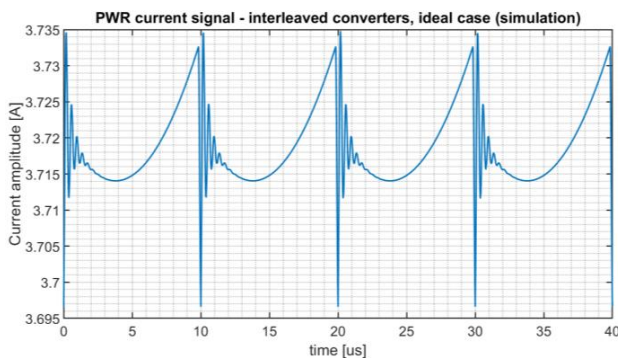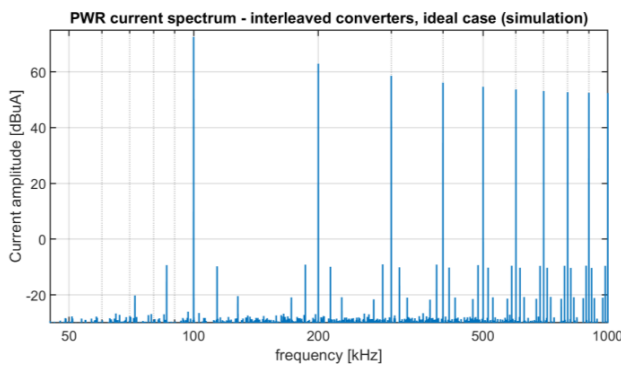
If more than 50 ns delay is added to the 10 µs time difference, then the input current ripples of the converters will not be in anti-phase in every period. This extra delay can be attributed to the improper phase-shift caused by the different turn-on times of the switches [10]. In Fig 5. we can see that the current ripple cancellation occurs only every 20 µs. The effects of this extra delay may be mitigated by differential mode (DM) filtering applied between the Power (PWR) and Return (RTN) (see Fig. 1) lines. In Fig 6. we can see, that due to the 20 µs time period the noise appears on the 50 kHz switching frequency and on its upper harmonics. From the measurements we will get similar results in time-domain as well as in current spectrum.

It is possible to set the time difference between the driving signals to zero (Δφ = 0°). In Fig 7. the resulting (PWR) line current signal can be seen. In this case the converter switch-on times are synchronized and their input current ripples are summarized in-phase on the PWR line.
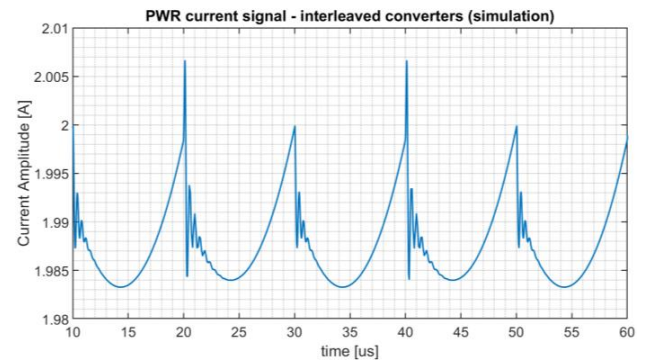

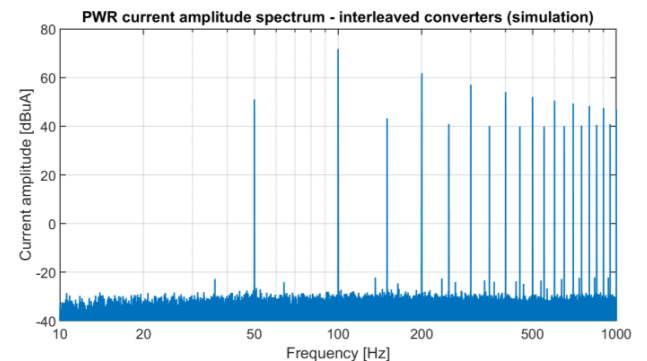Fig. 5 PWR current signal – interleaved converters, nonideal case, simulation results

Fig. 6 PWR current amplitude spectrum – interleaved converters, nonideal case, simulation results
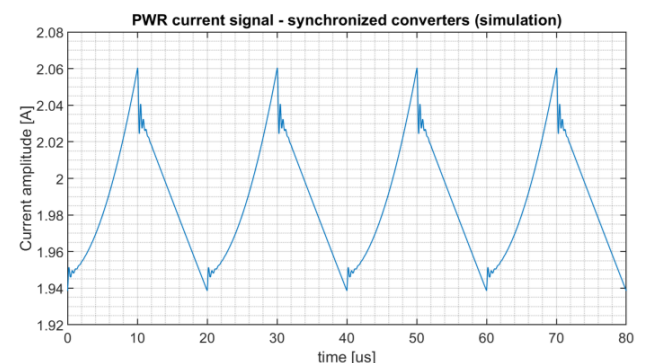

Fig. 3 PWR current signal – interleaved converters, simulation results

Fig. 7 PWR current signal – synchronized converters, simulation results

Fig. 4 PWR current amplitude spectrum – interleaved converters, simulation results
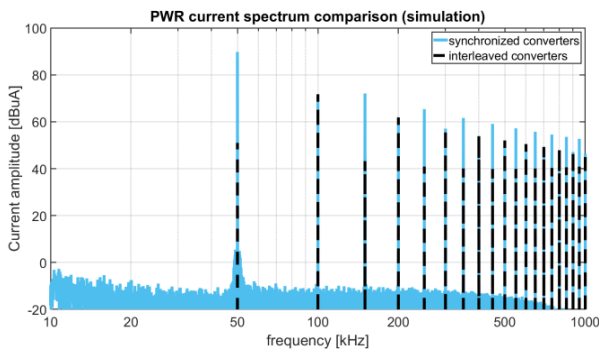
Fig. 8 PWR current spectrum comparison, simulation results

In Fig 8. we can compare the amplitude spectrum of the synchronized and interleaved converters. From this figure we can conclude that the noise component on the 50 kHz and on its odd upper harmonics (150 kHz, 250 kHz, 350 kHz…) is greatly reduced, especially on the switching frequency. The even upper harmonic components (100 kHz, 200 kHz, 300 kHz…) are amplified in case of the interleaved converters but due to the filtering of the LISN they mostly remain the same as in the case of synchronized converters. In these simulations we wanted to examine the effects of the interleaving directly and because of this we did not apply any filtering on the PWR and (RTN) lines excluding the LISN. In the next chapter we are going to present an EMC measurement setup with the same structure and the measurements described above will be conducted.

III. INTERLEAVING METHOD MEASUREMENT

For the measurements two Buck converters and a dedicated signal generator circuit was designed and built with the specification mentioned in the previous chapter. The block diagram in Fig 9. shows how the circuits are connected. For the regulation of the converters LM3524 Pulse Width Modulation (PWM) [11] control ICs were selected. The IC oscillators were synchronized by the outputs of the signal generator. With this setup we can set the phase angles of the converter switch-on times. The two major possibilities are the interleaving ($\varphi 2 = 180°$) and the synchronization ($\varphi 2 = 0°$) of the converters, but the phase delay can be set between these two values (see SYNC 2 in Fig 9.).

In Fig 10 we can see the entire EMC measurement setup. The LISN in this setup has the same structure as the one used in the simulations. The current signal of the PWR line was measured with a DC current probe, which was connected to an Agilent oscilloscope. The measurements were taken in time domain and later they were converted into spectrum with the FFT function of the oscilloscope [8]. The signal generator was fed from a different source and as it can be seen from Fig 9. the outputs were galvanically separated from the converters. In Fig 11. the assembled EMC measurement setup is shown.

The conducted emission of a switching mode power supply (SMPS) can be broken up into two major components: differential mode noise and common mode (CM) noise. The EMC ECSS standard contains regulations for both [7]. We are going to use these regulations to compare the measured current amplitude spectrum. The spectrum was examined only between

DC and 1 MHz due to the limitations of the oscilloscope, but an SMPS with a 50 kHz switching frequency can have noise components in a 100 MHz bandwidth. However, as we have seen previously from the simulations it is possible to make estimations from these measurements too [9].
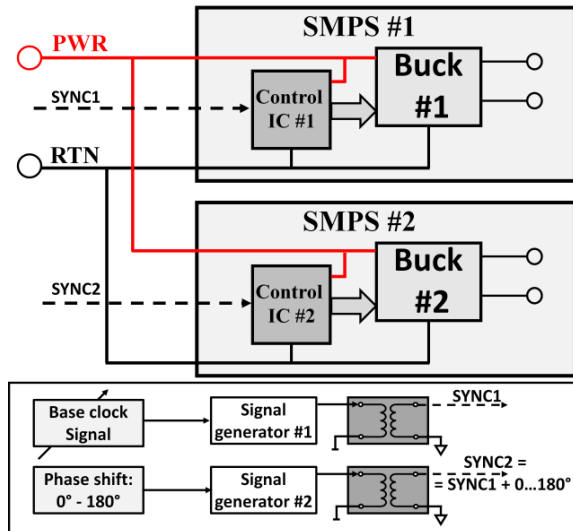

Fig. 9 Block diagram: Buck converters with the signal generator
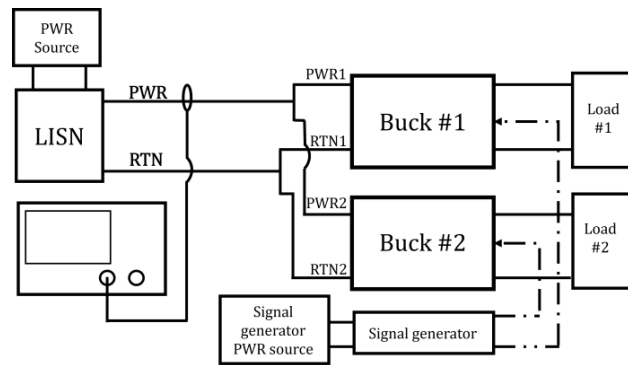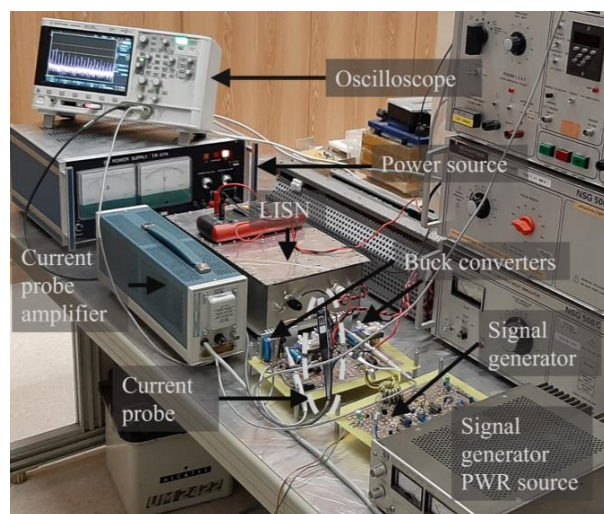

Fig. 10 Block diagram: EMC measurement setup

Fig. 11 EMC measurement setup assembled

The current amplitude spectrum measured on the PWR line can be seen in Fig 12. The spectrum was measured in case of interleaved and synchronized converters. From the measurements we can come to the same conclusion, as in the case of simulations: the noise on the 50 kHz switching frequency and on its odd upper harmonics are greatly reduced and the even harmonic components are mostly on the same level as in the synchronized case. These statements are depicted in more detail with the column diagrams in Fig 13 and Fig 14.
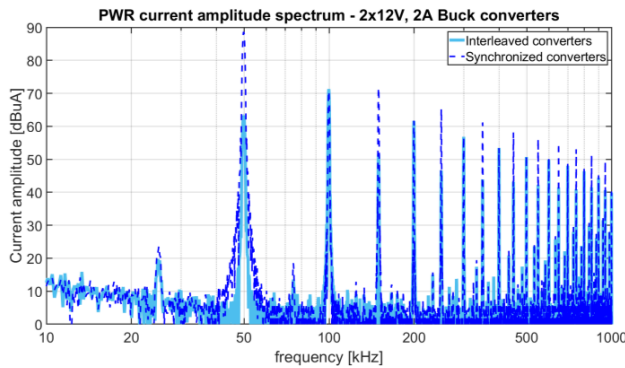

Fig. 12 Current amplitude spectrum measured on the PWR line
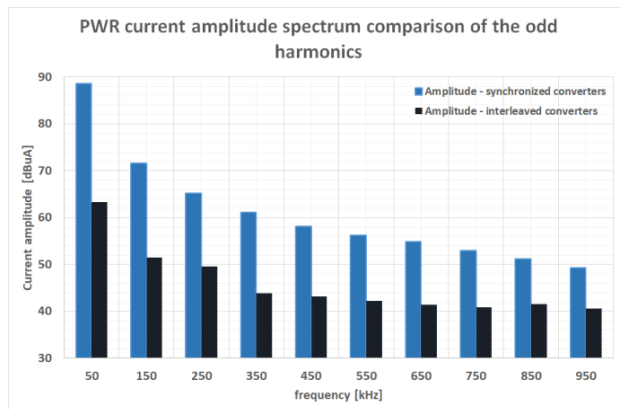

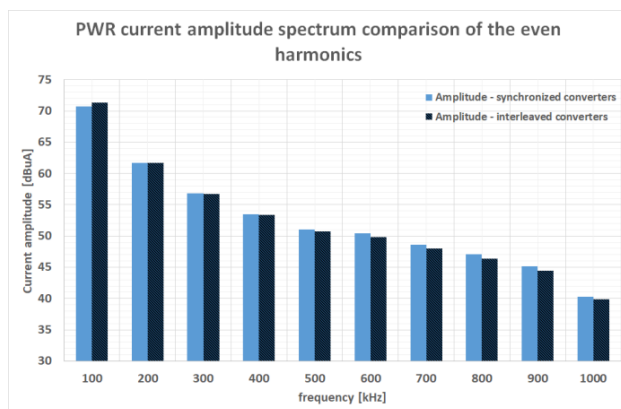Fig. 13 Measured current amplitude spectrum comparison of the odd harmonics

Fig. 14 Measured current amplitude spectrum comparison of the even harmonics
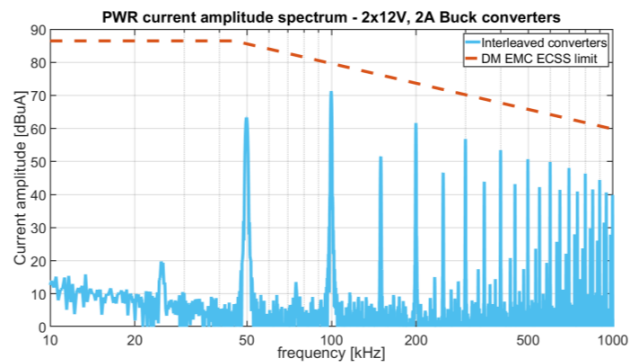

Fig. 15 Measured PWR current amplitude spectrum compared to differential mode limit (ECSS standard [7], p. 107, Fig. A-1)

The odd harmonic differences in Fig 13. are getting smaller as the frequency increases, because the amplitude of the components decreases exponentially in both control methods. The highest attenuation (25 dB) is achieved on the switching frequency, and on the 19th (950 kHz) component is around 9 dB. In Fig. 15. we compare the amplitude spectrum measured on the PWR line in case of interleaved converters against the differential mode limit issued in the ECSS EMC standard [7]. The measured PWR current spectrum is below the permitted level. The noise on the even harmonic components can be further filtered out with a capacitor between the PWR and RTN lines. Due to the strong attenuation of the switching frequency (and its odd harmonics), it is sufficient to filter the even harmonic components, which can be managed with a smaller capacitor value.

IV. Conclusion

In this article we examined the noise reduction effect of the interleaving method in case of a system with two DC-DC Buck converters. From the measurements we concluded that the switching frequency component and its odd harmonics can be decreased greatly, but not entirely. In the simulations we could recreate similar results by taking into account conditions, which make the systems non-ideal: component value tolerance, non-matching driving signal duty cycles and improper phase-shift. However, there are other factors, which may influence the noise reduction of the interleaving method. On-board of a satellite the payloads often require different voltages to function, but here we only studied two Buck converters with the same output voltages. If the output voltages are different, then the duty cycles and the peak-to-peak values of the input current ripples will be different. In such systems we can optimize the phase delay of the converters to improve the noise reduction of the interleaving [3].

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