5 Multiwavelength Sub-THz Sensor Array with Integrated Lock-In Amplifier and Signal Processing in 90 nm CMOS Technology

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CONTENTS

5.1 INTRODUCTION

The architecture and the operation of a sub-THz sensor array are presented, which has been implemented in standard 90 nm complementary metal-oxide-semiconductor (CMOS) technology. The integrated sensor array is arranged around 12 silicon field effect plasma wave detectors with integrated planar antennas. The received signals are further processed by preamplifiers, analog-to-digital converters, and a time-shared digital domain lock-in amplifier. The system automatically locks to external modulation and provides standard digital streaming output. Instead of building a uniform array, seven different antenna types with various polarization properties (horizontal and vertical linear, left- and right-handed circular polarization) and spectral responsivity have been integrated. The sensors altogether provide broadband response from 0.25 to 0.75 THz. The peak-amplified responsivity of the sensors is 185 kV/W @ 365 GHz, and at the detectivity maximum the noise equivalent power (NEP) is near $40\,pW/\sqrt{Hz}$. Relying on the drain current-induced responsivity increment, this peak value rises above 1.2 MV/W with a moderate $NEP \sim 200\,pW/\sqrt{Hz}$ at 50 nA source-drain current. Two application examples are provided as well: a multiwavelength transmission imaging and a homodyne imaging case with complex amplitude recording.

The THz spectrum of electromagnetic waves is nonionizing and has a broad application area [1]. In [2] Dyakonov and Shur predicted that the instability of electron plasma waves in short-channel field effect transistors (FETs) could be used as a terahertz frequency radiation detector. A different, more phenomenological description is given in [16] based on resistive self-mixing. Several THz imaging systems and different sensor technologies appeared, among others, silicon-based field effect transistors [2–6]. It found that not only high-mobility devices, but also silicon-based detectors with integrated planar antennas could serve as fast imagers as well [9, 10, 15–22]. The silicon- or SiGe-based sensor technologies offer an advantage over other material-based solutions, like bolometers, the on-chip integration of readout and signal processing circuitry [15]. Related to FET detectors, we can distinguish two basic operation modes: open drain and nonzero drain current cases. The former provides higher sensitivity, while the latter provides a significantly higher response [7], though with dominant flicker noise. In homodyne and heterodyne mixing FET detectors are presented [4, 12] with outstanding performance, similar to what Schottky diodes offer. These results suggest that still further improvements are expected from silicon-based sensors.

As the photodetectors advanced from a few passive pixels to single-chip video cameras, the same level of integration can be easily imagined for THz range imagers

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as well. This work is a step toward integrated imagers, by the inclusion of digitalization, digital postprocessing, and output streaming along the high-sensitivity and versatile sensors.
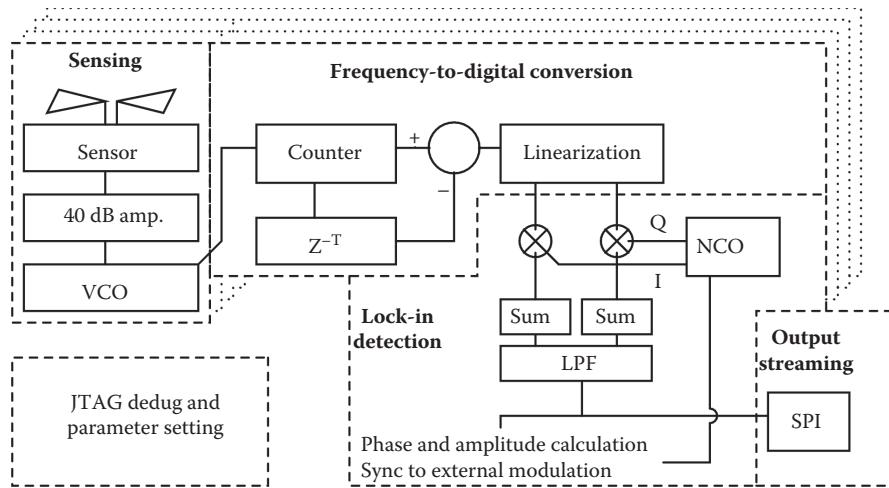
5.2   SYSTEM ARCHITECTURE

The presented sensor array contains 12 antenna-detector pairs and the following analog and digital circuitry. The system has been designed and manufactured using standard 90 nm TSMC technology. The motivation behind the system development is to investigate various antenna configurations operational from 0.25 to 0.75 THz and create an integrated smart pixel array for autonomous image acquisition.

From an engineering point of view, during the design with FET plasma wave sensors some fundamental difficulties should be addressed. One of the issues comes from the nature of the FET detectors [6]: the output signals (potential difference generated between the source and drain terminals) of the sensors are small ($\mu V-mV$). The typically subthreshold operation of the FETs provides low driving capability with output resistance of $k\Omega-M\Omega$. Hence, there is also a need for signal amplification with low input capacitance near the detector. This high output impedance results in relatively low-frequency operation into a region where the $1/f$ noise becomes significant. The detector's major noise contribution in open drain mode originated in its thermal noise across the channel, of which the power spectral density varies from a few dozen $nV/\sqrt{Hz}$ to $\mu V/\sqrt{Hz}$ for typical detector solutions. In nonzero drain current mode, the additional flicker noise further increases this value [7]. Though the sensor noise may rise to high values, the signal amplification must not add excess noise to the detector signal. These properties pose a practical limit on the amplifier design. The next problem to be solved is the free space coupling of the radiation to the detectors as the coupling determines the final performance. In standard silicon technologies the doped substrate constitutes a high loss factor and the metallization (number of metal layers, thickness, dielectric) is predetermined. As a result, resonant structures with ground shielding are relatively straightforward to design [34], while high-sensitivity broadband receivers are more difficult without microelectronic postprocessing (e.g., cavity etching under the antenna structure [17]). Finally, the high-impedance detector signals are susceptible for digital noise coming from other parts of the system, which requires careful mixed-signal design practice.

5.2.1   FUNCTIONAL STRUCTURE

The chip comprises 12 sensors arranged in a 4 by 3 array [21, 22]. The sensors are composed of an antenna-coupled FET detector followed by low-noise amplification. Next, each amplified sensor signal is digitalized and demodulated by a digital lock-in amplifier. The FET detectors are identical in each channel, while the antenna structures are different, including spiral, bow tie, and dipole antennas. For signal amplification an AC-coupled single-ended operational amplifier has been

FIGURE 5.1   System architecture. Components are antennas, detectors, low-noise amplifiers, VCOs and following frequency estimation, linearization modules, and common time-sharing lock-in detection comprising low-pass frequency filtering, numerically controlled oscillator (NCO), and output streaming.

integrated for each sensor. The digitalization is achieved by a voltage-controlled oscillator (VCO) and frequency estimation pair with calibration. The digitalization is followed by channel-wise lock-in detection. The implemented lock-in detection is based on amplitude modulation of the irradiation (or sensitivity modulation of the detectors) and complex-valued demodulation of the amplified sensor signal. There are two modes available: when the system provides modulation for the external radiation source and a complementary mode, and when it can synchronize to an external modulation coming from, e.g., a mechanical chopper. The demodulated responses of the channels are then low-pass filtered and selectively sent over an SPI port. The debug capabilities of the system are broad and reachable through a JTAG interface. The conversion parameters, the modulation frequency, and the low-pass filter parameters can be set via this interface. The reason for embedding a JTAG control interface is to reduce the pin count of the chip and to provide a simple and structured way to access its hundreds of control bits and internal states. The system functional architecture can be seen in Figure 5.1. The details of these functionalities and physical architectures are described in the following.

5.2.2   Optical Considerations

One could involve another constraint in the sensor array design as well: the optical properties of the system as an imager. In the presented system, instead of pursuing classic imager style operation, the focus has been moved to multiwavelength operation with polarization variants. The reasoning behind this follows.

On tabletops and short distances the THz imagers, including pulsed photo-conducting architectures, usually mechanical scanners, move the field of view or the object to collect the information from pixel to pixel or for a small pixel array. Most of the imaging platforms are built around reflective components in order to shape broad spectral range equally (e.g., broadband sources radiate in the 0.3–3 THz range). As a consequence of reflective optics, with a few additional refractive elements, the achievable focusing capability is restricted. The reported numerical apertures vary from 0.4 to 0.05, resulting in a 2 to 10 times larger spot size than the actual wavelength. Due to the resonant antenna size reduction implemented in a substrate, the optimal antennas are typically much smaller than what the optics can resolve. In other words, the effective area of a single antenna with matched resonant peak is much smaller than the reasonable spot size. Taking a practical example of a focal plane detector on silicon substrate, the difference between the optical resolution and the antenna size could be an order of magnitude. Using an *f*/1.4 optics and operational frequency at the water absorbance peak at 0.55 THz ($\lambda = 0.55$ mm), the optimal dipole antenna length would be 108 μm [36], while the spot size FWHM diameter becomes about 1 mm ($D = 1.22\lambda_0 f_{\#}$).

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One can find solid immersion lens solutions in a form of silicon elliptical or hemispherical lenses [24, 25]. On the other hand, these solutions have a substantial decrease in amplitude at high frequencies and strong frequency dependence [23]. Another way is to integrate many individual sensors in a multichip module [25] to mitigate the large difference between antenna size and free space wavelength.

5.2.3 Physical Architecture

The physical floorplan is determined by the sensor array. The antennas require definite area, while the digital and analog circuitry could be placed practically in any shape and aspect ratio. First, the targeted frequency range is selected (0.25–0.75 THz) and the main structural dimensions of the antennas are calculated. Seven different antenna structures are designed with different polarities based on knowledge of the technological fundamentals, such as metal layers, their thickness, and dielectric properties. Next, using the antenna dimensions, mutual crosstalk requirements, and distance from the package wire bonding, the unit cell is fixed and the available area is divided into 12 such cells of equal size with a pitch of 330 μm. The digital circuitry takes place on a distant corner and the analog front-end circuitry is integrated within the sensors with careful EM shielding. The resulting floorplan is presented in Figure 5.2.

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In order to make the design phase more efficient, each cell has exactly the same circuitry and layout, except for the antennas. This way, antennas of different kinds are placed in a similar metallic environment and the circuit design and verification are simplified greatly. The cell layouts are placed rotated and mirrored to share power distribution lines and to save area by overlapping metal-insulator-metal (MIM) capacitor bounding structures. The concept can be seen in Figure 5.3.
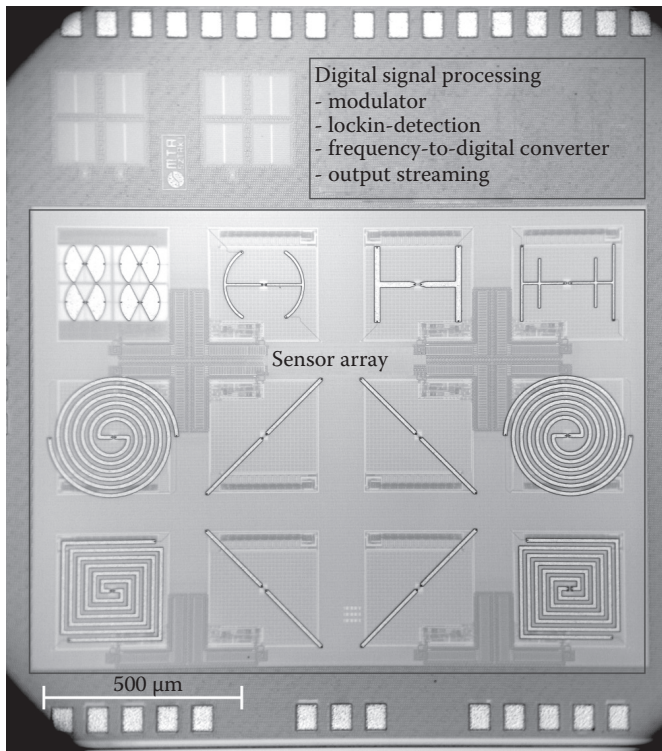
FIGURE 5.2   ASIC microphoto showing the system floorplan and the variety of antenna-coupled sensors.

A constraint must be taken into account; namely, the commercial CMOS technologies are built on conductive, lightly doped silicon substrate. The antennas directly implemented on such a substrate suffer from high substrate losses. A trivial solution is to create a metal shielding beneath the antennas and right on top of the substrate. Thus, in order to avoid high substrate losses, each antenna is placed on the top metal layer with a ground metal mirror underneath in the lower metal layers. One exception to this rule is the sensor of the bow tie antennas. The reason is that the other types are resonating at specific frequencies, while the bow tie antennas are designed to be broadband. Though it responds as expected, its sensitivity is below the resonating and shielded ones, and as shown later, the response is significantly altered from the theoretical one due to substrate resonances. More precisely, as Figure 5.3 illustrates, the substrate is covered by a ground shield formed by the two lowest metal layers (MET1–2). The reason for the double layer is that the signal paths reaching the detectors in the middle of the cells are also covered this way: they run in the lowest metal, while the second metal remains intact. The next structural element is another shield layer created on a higher metal layer, namely, in the sixth one (MET6). This shield covers the majority of the circuitry and is placed at the border of the cells. This layer is also used for power distribution. At last,
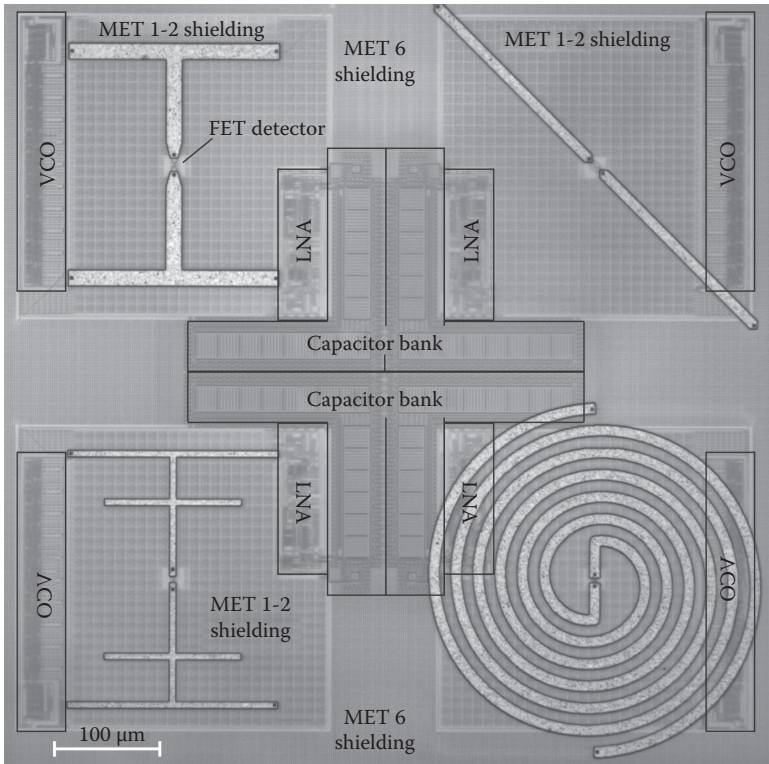
FIGURE 5.3   Floorplan of four adjacent sensor cells with their main components.

another role of this shield is to embed the selection and other signals coming or going to the digital region in the intersensor channels. The antennas are formed on the top metal layer. This particular technology offers nine metal layers for routing, with thicker ones on the top, and an additional thick layer, called the power distribution layer, of 3 µm above the routing layers. From an EM design point of view, the height of the antenna structure above the ground shield is advantageous to increase; hence, the top layer is picked for the antennas. Near the FET detectors, the lowest metal shields are opened and a staggered structure has been built from lower metals and vias. The exact structure affects the behavior of the antennas and needs detailed EM simulation to maximize the electric field concentrated on the detector FET. The illustration of the role of the different layers is shown in Figure 5.4.

5.3   FREE SPACE COUPLING

The FET detector sensitivity and operation are determined by the manufacturing technology and materials (e.g., minimal feature size, silicon or compound material, etc.) and do not alter significantly across the same feature-sized CMOS technologies
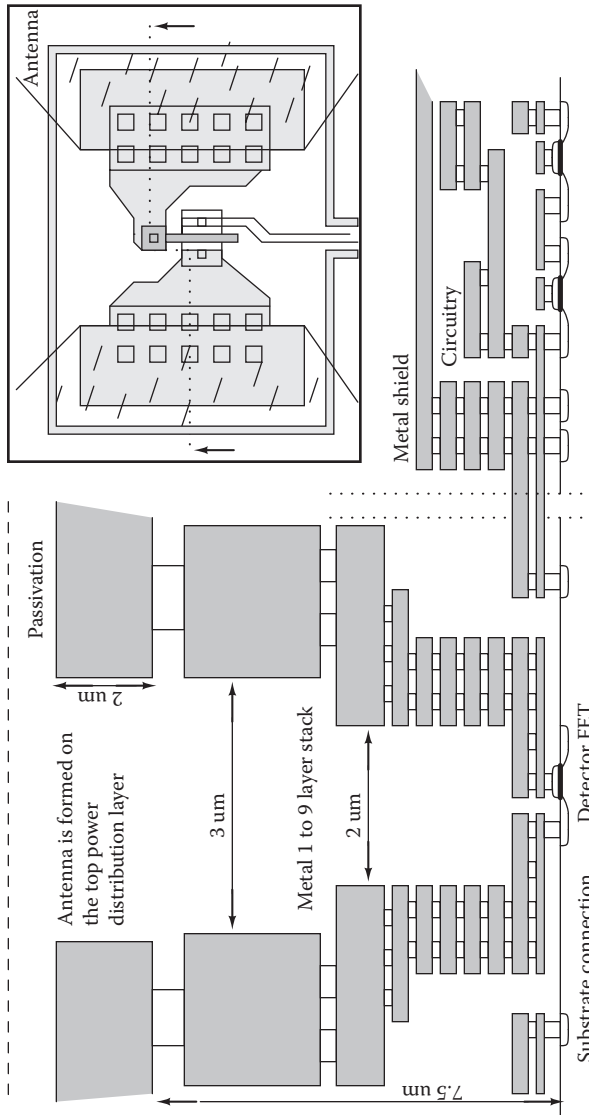
FIGURE 5.4 The metallization strategy near the detector FETs and the nearby circuitry shielding can be seen. The upper right inset shows the bird's-eye view of the detector connection layout to the antenna wings.

[10, 12, 18]. On the other hand, what crucially affects the overall sensitivity is the antenna design and coupling strategy. The basic element of radio frequency (RF) microelectronic technologies is the integrated planar antenna. In the design of an integrated antenna one can choose broadband (e.g., bow tie) or narrow band (e.g., patch) antenna types from the numerous implementation styles [33–35]. The implemented antenna variants are easy to identify on the microphoto in Figure 5.2 and are the following:

- Dipole of different polarization directions (resonate at 0.25 THz)
- H-shaped dipoles (resonate at 0.36 and 0.45 THz)
- Two-armed Archimedean and squared spirals (with 8 and 10 significant resonant peaks from 0.15 to 0.5 THz, respectively)
- Serially connected bow tie antennas on silicon substrate (with peaks at 0.44, 0.55, and 0.7 THz)

The antenna design follows classic methodology. First, the spectral response is selected and the type of antenna (bow tie, spiral, dipole, H-shaped dipole). Next, based on the technology parameters, a quick, textbook estimate is calculated [35]. The responsivity peak(s) of the antenna could be estimated by a simple quasi-static approach up to 1.5 THz according to [36]. At last, an EM field simulator is used to find out exact dimensions, still using ideal metals and a dielectric structure. The actual layout further changes the ideal EM simulation result, caused by slotting design rules and the quantized shape of the vias. This alteration can be verified and fed back to the sizing by exporting the layout from the CAD tool and importing it into the EM simulator. As a last step, the design of the detector coupling is optimized from an electromagnetic point of view with the EM field simulator and simplified plasma wave detection modeling [9]. As a distinguishing step from the classic antenna design, the electric field strength is maximized on the FET terminals, instead of relying on the S-parameters.

5.4 MIXED-SIGNAL INTERFACE

The analog interface design covers the analog front end and the digitalization. In the front end, the requirements are derived primary from the FET detector behavior: the high output impedance, band-limited modulation frequency, and near-ground small signal values. The choice was an AC-coupled single-ended amplifier with low cutoff frequency and small input capacitance. As an additional feature, a simple way is provided to characterize a nonzero drain current configuration. The circuitry details are described next.

5.4.1 Analog Front End

The FET detector sensitivity increases, lowering the gate-substrate voltage due to the electron plasma thinning under the gate electrode [5]. The downside of this sensitivity increase is that as the transistor penetrates deep into subthreshold, the output signal becomes vulnerable to thermal noise and the FET's output impedance

rises exponentially. The basic solution is to terminate its drain with a high-value resistor toward ground level and measure the potential appearing on this resistor, or to inject nonzero DC source-drain current and measure the voltage drop on the detector. In the latter mode, the responsivity of the sensor significantly increases, though the sensor flicker noise increases as well at almost the same rate as presented in [7] in case of high electron mobility transistors. In order to get rid of broadband noise, usually radiation modulation is applied, along with a lock-in amplifier. This way the 1/f noise can be efficiently suppressed as well. Hence, the analog signal conditioning must have low input capacitance (~pF) to allow adequate modulation frequency to avoid low-frequency noise. The open drain detectors produce near-ground-level signals, so capacitive coupling had been chosen to get rid of the low DC signal.

The signal amplifier is motivated by neurobiological solutions, due to the similarity of low signal levels and low-frequency modulation [27, 28]. The implemented circuit provides 40 dB amplification with 250 Hz to 0.5 MHz lower and upper –3 dB cutoff frequencies. The amplifier has a folded cascaded structure with a PMOS input transistor (Figure 5.5).

It has a small footprint and moderate noise contribution (~40 nV/√Hz at 1 kHz input referred noise), which is smaller than the FET detector thermal noise in its high-sensitivity region. In order to minimize the substrate noise, the detectors and the amplifier are protected by deep n-well guard rings. The band pass filter is based on the high-resistance pseudoresistor and metal-oxide-metal capacitor. The higher frequency limit comes from the lock-in-oriented operation, i.e., physical light chopper and radiation source modulation frequency. The lower cutoff frequency is intended to suppress the increasing 1/f noise of the amplifier. Note that the operational conditions of the FET detector at its noise equivalent power (NEP) minimum also limit the upper modulation frequency to about a few kHz. The band pass amplifier topology can be seen in Figures 5.6 and 5.7 for the single and multiple detector configurations.

The FET detector can be considered part of the analog front end. The detectors are identical in each pixel and have drawn a size of W/L = 500 nm/100 nm. The detector transistors are connected so that the gate is fed by an antenna wing; their drain is connected to the other antenna wing and the DC shortened to ground, while the source side feeds the amplifier. This particular connectivity produces negative source-side signals [17], which are inverted by the amplifier topology. In order to support a nonzero drain current configuration, a PMOS-based pseudo-resistance of high nonlinear resistivity is integrated. The pseudoresistance behaves as a linear resistor (in the range of GΩ to TΩ) at low potential difference between its terminals [27]. On the other hand, its conductance increases significantly by increasing its terminal voltage (>0.7 V). Connecting to the FET detector, it allows driving 0–5 µAmp source-drain current, which can be set and monitored outside. Until the response of the detector remains in the mV range, the linearity, high value, and fine tunability of the resistance are maintained. The great advantage of this solution is that it has a small footprint, and has very low noise compared to any current source-based architecture.
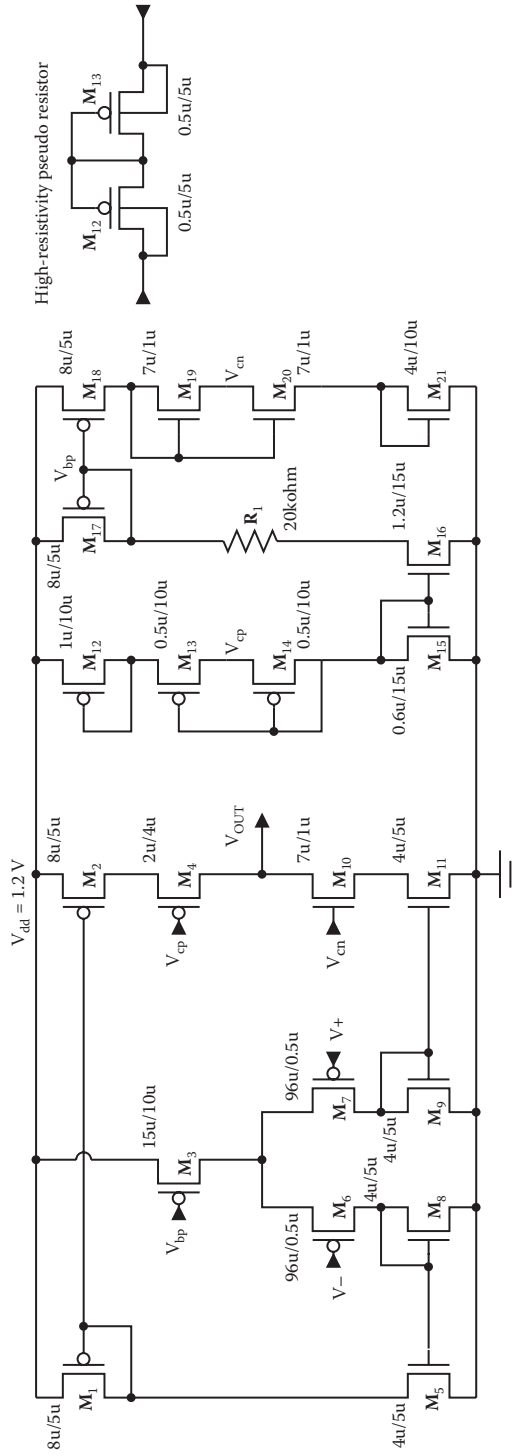
FIGURE 5.5   On the right side, the amplifier with biasing network is shown. In the upper left corner, the implemented pseudoresistor can be seen.
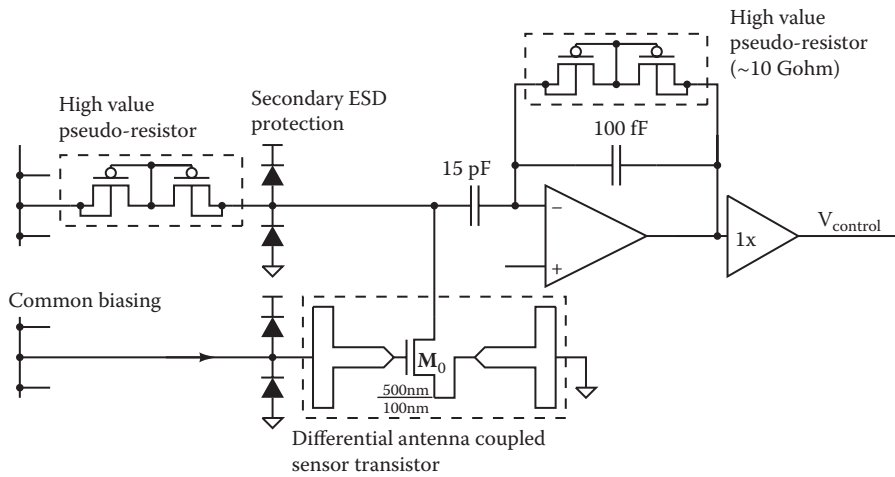
FIGURE 5.6 Simplified schematic of the H-shaped dipole antenna-coupled detector and the band pass amplifier.
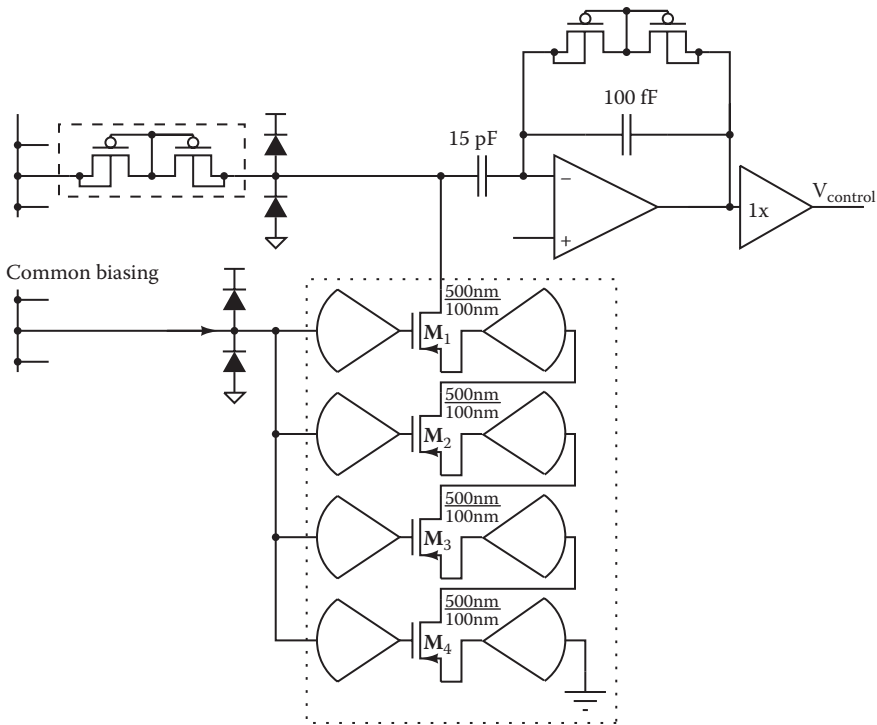

FIGURE 5.7 Simplified schematic of the serially connected multiple bow tie detectors and the amplifier.

Note the ESD protection on the detector ports as well. First, the reason for including such secondary ESD protection is that the gate signal is provided externally and the pad ESD circuitry is routed far from the sensors. Second, the large antenna area may alter the transistor gate threshold level during manufacturing in an unpredictable way (so-called antenna rules are met this way).

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5.4.2 DIGITALIZATION

A free-running VCO and a frequency estimator generate digital representation of the amplified sensor response. The reason for this choice is the limited layout area and metallization that restricts the ADC complexity, and the voltage-to-frequency converter has a small footprint with reasonable precision (25 × 230 μm). The VCO is based on a five-stage interpolating voltage-controlled delay line, which provides low jitter [29]. In order to reduce the clock feedthrough from the oscillator to the sensor via the capacitive amplifier, distributed source followers and a unity buffer are inserted. The VCO can be tuned by the variable capacitive load that supports a wide frequency range (180 ~ 260 MHz) centered at 230 MHz at the nominal half-supply voltage of 0.6 V bias and ±0.3 V control voltage swing. The VCO architecture is shown in Figure 5.8 and a single stage of the ring oscillator is presented in Figure 5.9.

The frequency of the VCO is first divided by two at the VCO to obtain 50% duty cycle and measured by a counter, whose increment is sampled by regular time periods. In addition to the static nonlinearity, differences arise in the oscillation frequency of the VCOs due to manufacturing inaccuracies. These effects are compensated after digitalization by a second-order polynomial equation. This plain ring oscillator is sensitive to temperature and power supply changes as well. It is placed on a separate power domain, which is supplied by an external LDO with high-voltage stability.
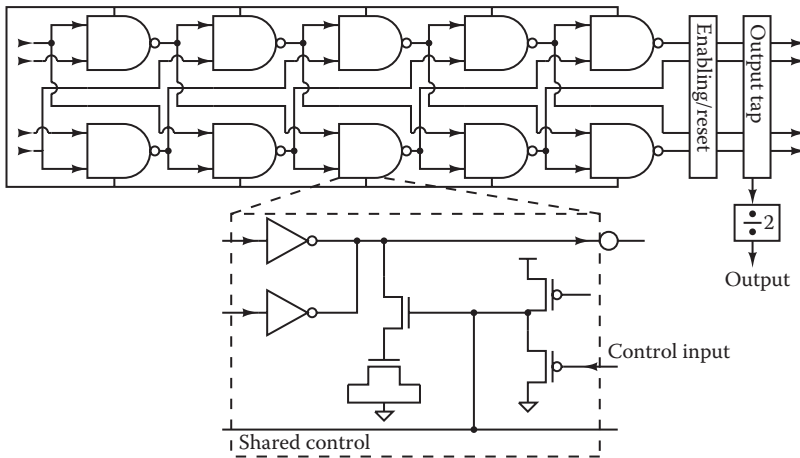

FIGURE 5.8 The implemented low-jitter voltage-controlled delay line with kickback-reduced control input. Its output is fed back to its input to form a voltage-controlled oscillator.
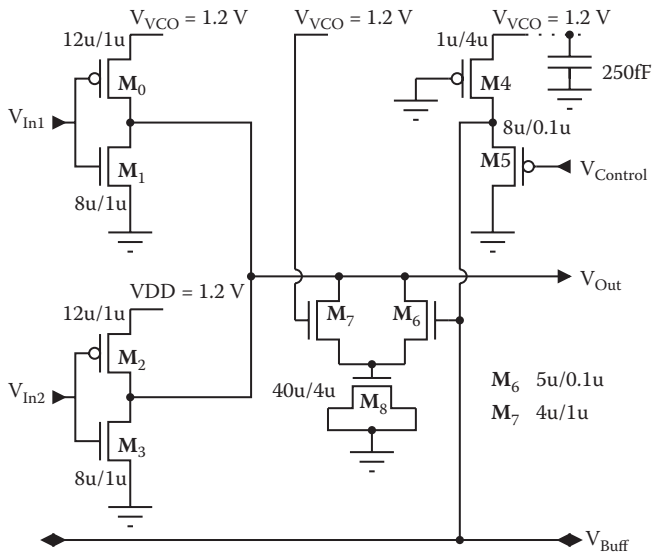
FIGURE 5.9   One stage of the voltage-controlled delay line.

The temperature dependence is handled by repeated measurement cycles using the test access points before actual measurements, and its results are incorporated time to time into the compensation formula. The corrected 24-bit fixed-point output values (8-bit fractional) are sent toward the lock-in detection. Under nominal operating conditions, the small signal conversion factor of the VCO is 125 *MHz/V* with a tracking jitter near 350 ps. Though it is a high value for jitter, taking the practical timing conditions of pixel acquisition into account, the overall performance does not deteriorate the results significantly. The VCO uncertainty at a 1 KHz conversion rate yields approximately 0.03 *MHz* frequency estimation standard deviance. Supposing 1 and 10 pixels per second acquisition rates, it would correspond to 70 and $230nV/\sqrt{Hz}$ detector-referred noise.

5.5   DIGITAL CIRCUITRY

The digital circuitry is responsible for handling the streaming data coming from the 12 sensors and maintains communication with the external host. The reason for the inclusion of such functionality into the system is straightforward: make the operation simple and versatile. The implementation style was standard digital flow based on manufacturability, testability, and low-power standards.

5.5.1   CONTROL AND MONITOR

The check and control of the digital part of the system is twofold: first, its correct operation is verified; second, its operational parameters are set. In order

to balance the chip area overhead and testability, only specified points are monitored and substituted in the data flow. The test development, including test generation and fault simulation and coverage, has been conducted. The fault-free response is checkable by binary vectors at the monitored buses and CRC checksums. The settable parameters and the test points are chained in different domains of a standard JTAG controller, and the external pads are chained in a standard boundary scan [38]. The JTAG interface-handled chains are the following:

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- Analog block (including low-noise amplifiers (LNAs)) enabling register
- Analog/digital interface enabling register (including VCO control)
- Digital core configuration register (various parameters, such as modulation frequency, mode of locking, oversampling of the digitalization stage)
- Monitoring and substitution of the digitalization stages
- Analog access port control register
- Digital core, various output sample registers

5.5.2 Lock-In Detection

As usual in low-signal-level situations, the sensor responses are detected by the lock-in technique. This method increases accuracy and precision by acquiring information with modulated stimulus and integrating the samples over a large time period with low-pass filtering. Correspondingly, the core of the digital part is a digital lock-in amplifier. It consists of in-phase and quadrature phase demodulation, low-pass filtering, and data streaming modules (Figure 5.1). The digital lock-in detection is capable of locking to the source modulation frequency and provides the complex and absolute intensity of the input signal at the selected frequency bin. Besides this mode, the chip can generate a modulation signal as well.

The system performs signal amplification and digitalization per sensor channel in a distributed way, while the lock-in detection is done by a time-shared data path ALU. The ALU is a fixed-point integer with changing fractional and integer bit length. This module processes all sensor channels or a specific physically meaningful selection of them, while the nonused sensors are usually switched off by the JTAG interface. The simple formula of the complex-valued calculation in a single bin is as follows:

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$$Y_B^W = I_B^W + jQ_B^W = \sum_{n-0}^{W-1} X_{\text{sensor}}(n) * \exp^{\frac{i*2\pi}{W}*B*n}$$

where W and B denote window size and frequency bin, respectively. The real and imaginary parts (I, Q) are processed independently. The calculation of the single sensor is done by summing the product of the input time series with sin/cos waveforms representing the in-phase and quadrature phase. The waveforms are generated from a lookup table, which is part of a numerically controlled oscillator

(NCO). This NCO derives a fractional frequency from the main system clock and periodically provides the sin/cos values. The intensity value of a specific sensor y_{ch} is calculated then as

$$y_{sensor} = Y(\text{sensor}) = \frac{\sqrt{I_{sensor}^2 + Q_{sensor}^2}}{W}$$

The numeric representation of the sin/cos waveform is signed 12-bit with 11-bit fractional, the I, Q values have 36-bit with 11-bit fractional, and the output is 40-bit with 8-bit fractional. The final output data consist of the real and imaginary parts and the intensity value of the selected frequency bin. When a complete time window is ready, all results of the enabled channels are streamed out by a standard SPI bus.

5.6 TESTABILITY FEATURES

Besides the normal operation of the sensor array, there are numerous test requirements. Such requirements range from near-thermal noise measurement of the sensors under sub-THz irradiation to multichannel lock-in detection data path verifications. The system is prepared for these cases by JTAG-controlled fine-grade on/off power domains, digital access ports, and standard mixed-signal test solutions.

First, multiple power domains have been implemented. The reason is primarily to support clean power supply for the analog front ends and decouple the VCO high-frequency noise from the rest of the circuitry. The secondary motivation is to provide a noise-free environment for the FET detector characterization by completely switching off the VCO and digital regions. Though the antenna-coupled plasma wave detector behavior could be modeled to a certain complexity, the RF characterization of the sensors and the following LF signal path must be separate. The mixed-signal path verification and characterization is available by analog boundary modules [38]. These modules are placed in order to facilitate analog parametric characterization. On the other hand, if the FET detector alone is under test, it is useful to detach its, e.g., noise performance from the rest of the circuitry. There are a set of digitally controllable analog boundary cells implemented near the sensors: amplifier and VCO input and outputs can be selected for tests and disconnected from the signal path. Their signals are connected to analog test I/O pins. In a similar way, external input voltage is provided for the VCOs, whose outputs are directly accessible at an I/O pin as well.

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5.7 RF CHARACTERIZATION

The radiation source used is a YIG oscillator-driven VDI amplifier/multiplier chain (AMC) to generate an 80 to 750 GHz signal. The polarized signal is radiated through a horn antenna and collimated and then focused by off-axis parabolic mirrors. The responsivity has been calculated by raster scanning the spot size and scaling the beam power measured by a VDI Erickson absolute power meter to the integrated response [17]. The different antenna structures provide various frequency responses.

The resonant peaks are drifted in frequency and spread over the resonant peaks compared to the EM simulations. The following data are listed for the highest responsivity structures: the narrow band H-shaped dipole and broadband four serially connected bow ties [30]. The detector noise characterization is performed under a battery-powered setup with switched-off VCO, digital signal processing domains, and using external low data acquisition.

5.7.1 RESPONSIVITY

In the plasma wave sensor context, the RF characterization typically embeds a frequency-dependent response in conjunction with detector biasing. The biasing means VGS and IDS sweeps of the sensor transistor. Another important feature of such sub-THz sensors is the noise equivalent power, whose measurement requires a noiseless environment. The RF setup based on a sub-THz source is the ensemble of a YIG oscillator and a multiplier amplifier chain operating from 80 to 750 GHz. The irradiation power reaching the sensor plane is validated by a bolometric absolute power meter through a high-resistivity silicon (HRFZ-Si) beam splitter. The focusing is helped by a fiber-coupled visible diode laser and an ITO-covered glass mirror (see Figure 5.17). The quasi-optical setup enables automated modulation frequency, polarization, and attenuation control. These features are generated and the detector response is captured by a standard data acquisition system.

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The responsivity was measured according to [17]. This technique is based on raster scanning a focused spot and normalizing the received response with the beam power and the effective area of the detector:

$$R_{det} = \frac{U_{det}}{P_{det}} = \frac{\iint_{area} U_{det}(x, y)dx\,dy}{P_{beam} * A_{det}}$$

The responsivity can be calculated, where U_{det} is the DC photoresponse, P_{beam} is the total beam power in the detector plane measured with a large-aperture THz bolometer power meter, and A_{det} is the detector size. In [17] A_{det} is chosen to be the physical size of the detector, i.e., the pitch size. It is well known that an antenna receives the incident power density by its effective area. The effective area usually does not equal the physical area. In [16] the same scanning process was performed but interpreted in a different way, which is adopted here. Namely, they simulated the antenna's directivity and applied the following well-known equation:

$$A_{eff} = D \frac{\lambda_0^2}{4\pi}$$

where D is the directivity of the on-chip planar antenna and λ_0 is the free space wavelength. However, it must be emphasized that this expression is valid if and only if the used antenna is under the following conditions: (1) lossless and (2) impedance and polarization matched over the whole frequency band, where is it functioning.

Based on the formulated responsivity measurement, several aspects of the sensors can be characterized. As described in detail in [11], the loading effect is presented first. The responsivity is measured as a function of the source-gate potential and the radiation modulation. By these two parameters the maximal response can be found for a system, which is limited by the detector and the following resistive/capacitive loads, such as amplifier input capacitance and bandwidth. Figure 5.10 presents the results of the H-shaped antenna-coupled sensor behavior as a function of gate-source voltage and the input radiation source modulation frequency. Its frequency response is limited at low frequencies by the amplifier roll-off and at higher frequencies by the radiation source used. Nevertheless, the resulting curves suggest that the peak responsivity is near 190 kV/W at 1–2 KHz modulation frequency.

Next, the nonzero source-drain current effect is measured. The drain current increases the response of the detector [7] with the price of increasing $1/f$ noise. Fixing the modulation frequency at 1 KHz, the source-drain current effect is measured and shown in Figure 5.12. Figure 5.11 is presented as a reference for the source-drain current dependence on V_{PR}. The resulting curves are similar to the expectations, with the difference that the enlargement of sensitivity is lower than that found in the high electron mobility transistor (HEMT) case. In the case of this antenna, the largest responsivity values reached 1.2 *MV/W*. The drain current was injected by applying external voltage on the drain-side pseudoresistance. Its resistance decreases significantly, and lets current flow through the detector FET. The current is measured externally.

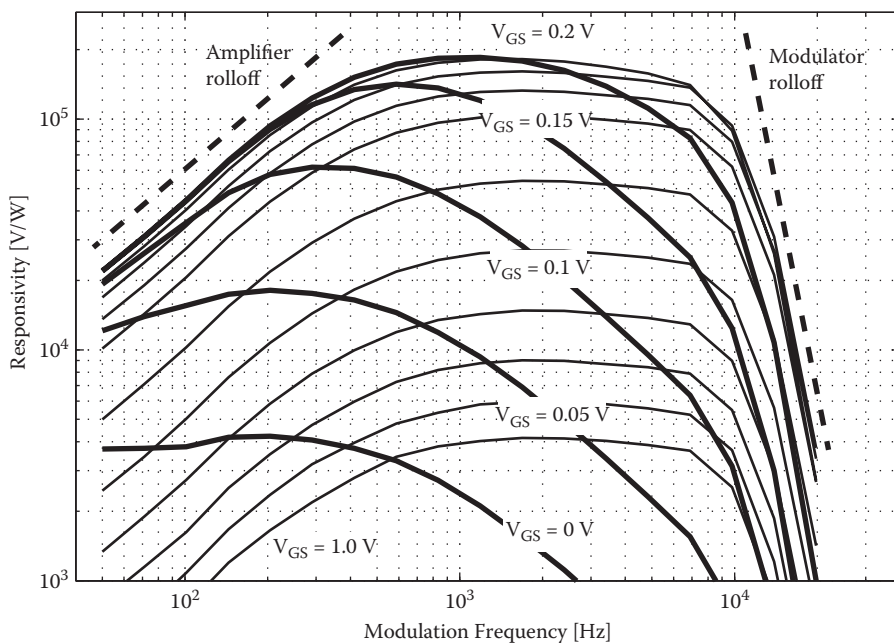AU: Figure in-text citations do not appear in sequence. Please check

FIGURE 5.10   The H-shaped dipole antenna-coupled sensor responsivity at 360 GHz as a function of gate-source voltage and the input radiation source modulation frequency.
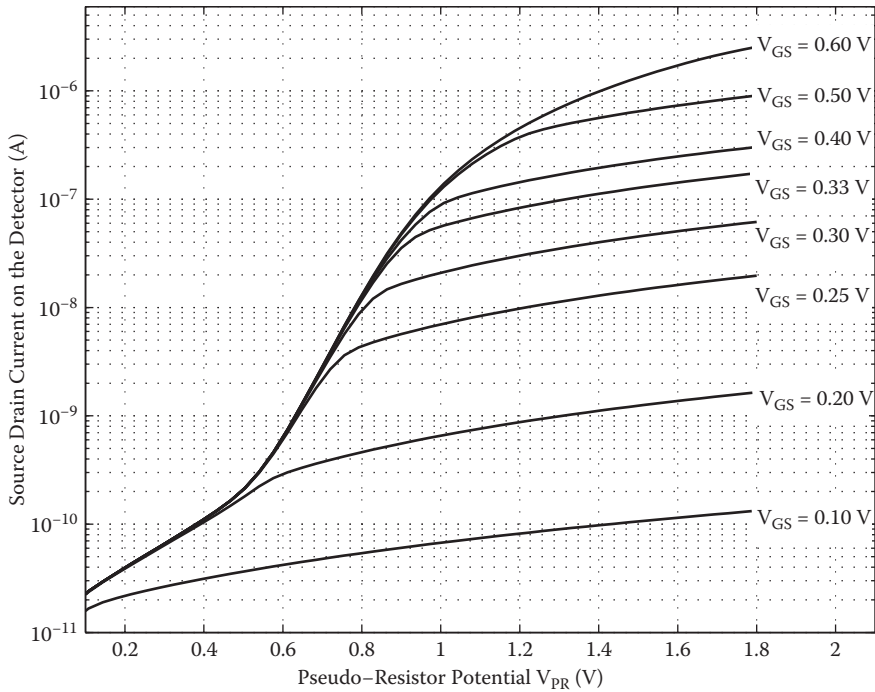
FIGURE 5.11   Source-drain current versus the gate-source voltage and the pseudoresistance potential.

5.7.2 Noise

The next important question is the noise performance. In an open drain configuration, the noise is dominated by thermal noise of the detector channel as $N_{det} = 4kT/G_{DS}$, where G_{DS} is the channel conductance at zero drain-source voltage. Additional noise sources such as noise due to the distributed substrate resistance and shot noise associated with the leakage current of the drain-source reverse diodes are neglected in this calculation. If current flows through the detector, the additional flicker noise appears, which is proportional to $1/f$ as $N_f = K_f/(C_{ox}^2, W, L, f)$, where W, L, C_{ox} are parameters of the transistor, and K_f is a technology-dependent constant [28]. Finally, the amplifier input-related noise is taken into consideration as $N_A(f)$. The noise equivalent power (NEP) is an important figure of merit that describes the minimum power detectable per square root of bandwidth, which is defined as

$$NEP_{system} = \frac{Total\ noise\left(\dfrac{V}{\sqrt{Hz}}\right)}{Responsivity\left(\dfrac{V}{W}\right)} = \frac{\sqrt{N_{det} + N_f + N_A + N_{ADC}}}{R_{det}}\left(\frac{W}{\sqrt{Hz}}\right)$$
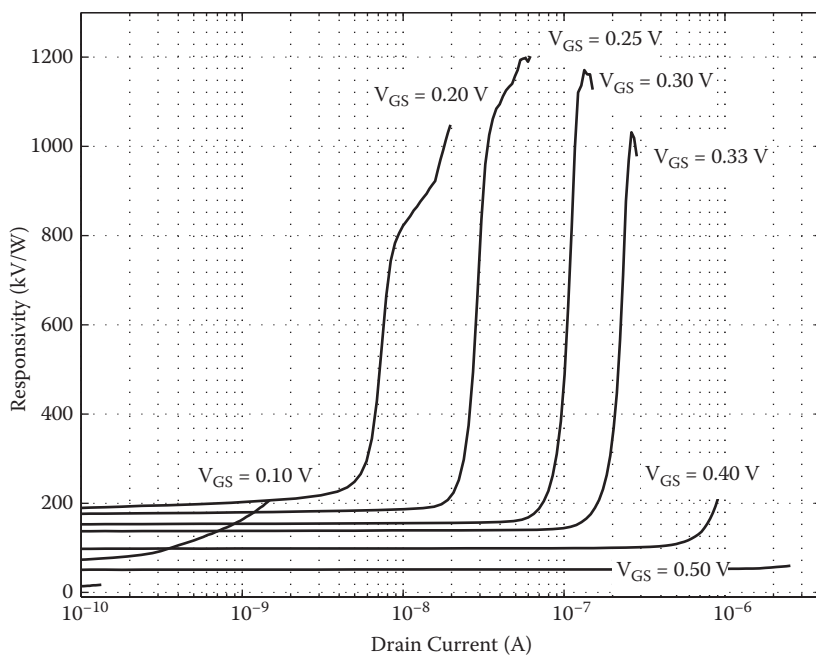
FIGURE 5.12   The H-shaped dipole antenna-coupled sensor's amplifier responsivity as a function of source-drain current injected through the pseudoresistance.

Figure 5.13 shows the NEP for different source-gate voltages as a function of the pseudoresistor potential (V_{PR}). What is important to note is that the NEP does not improve significantly at any point as the source-drain current increases, as found in the HEMTs. On the other hand, at $V_{GS} \sim 0.25V$ and $V_{PR} \sim 1.6V$ and $I_{DS} \sim 50nA$, the responsivity increases to the *MV/W* region with a moderately increased NEP value of about 200 $pW/\sqrt{Hz}$.

5.7.3 Design Examples

In the following, two particular sensors are described in detail: the bow tie and the H-shaped dipole antennas. The response and the design metrology are different for these basic types. The microphotos with the physical dimensions are shown in Figure 5.14.

5.7.3.1   Resonant Antenna

In general, the effective permittivity (ε_{eff}) of the substrate-air half spheres tunes the fundamental resonant length (L_R) of the antenna below compared to their free space counterparts (L_0):

$$\varepsilon_{eff} = \frac{\varepsilon_0 + \varepsilon_{substrate}}{2}, \ LR = \frac{L_0}{\sqrt{\varepsilon_{eff}}} \alpha \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}}$$
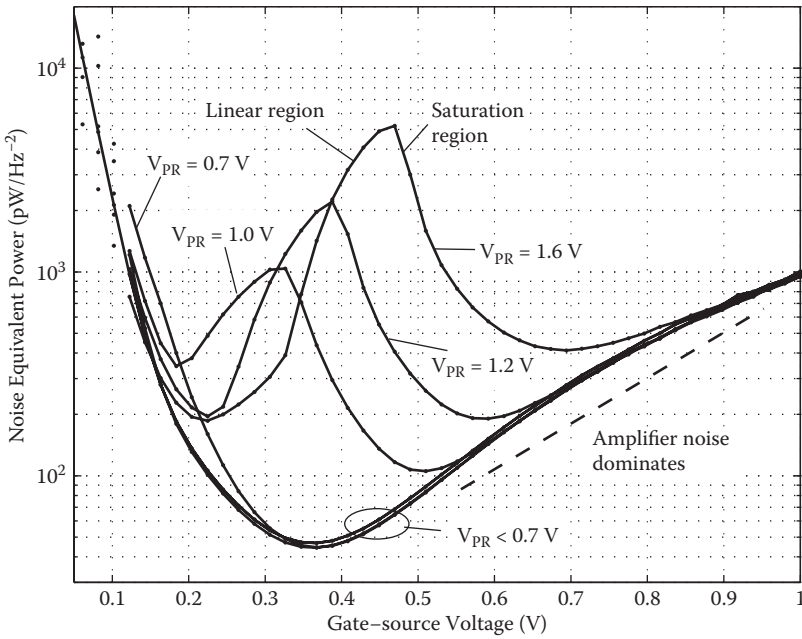
FIGURE 5.13   The H-shaped dipole antenna-coupled sensor's noise equivalent power at 360 GHz as a function of gate-source voltage and potential applied on the pseudoresistor load.
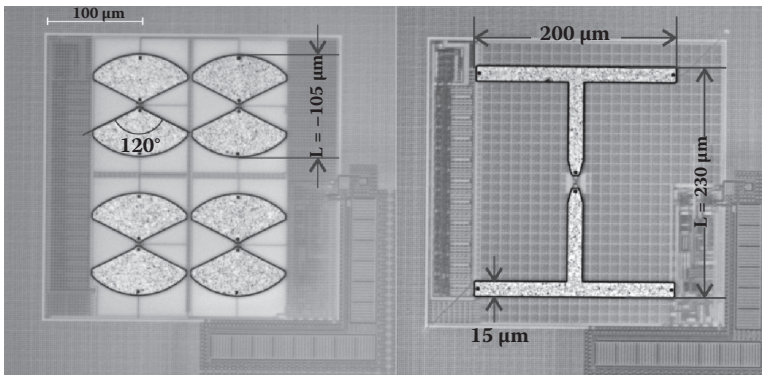

FIGURE 5.14   Microphotos of two specific sensors with broadband and narrow band responses: with bow tie and H-shaped dipole antennas.

   The resonant length of an antenna implemented on silicon substrate ($\varepsilon_{Si} = 11.69$) becomes 2.5 times smaller this way. In the mainstream technologies, the metallization is embedded into a sandwiched dielectric structure (combination of SiO_2 or low-K materials with dielectric constant $\varepsilon \sim 2, \ldots, 3.9$) and covered on the top as well (e.g., with Si_3N_4 with dielectric constant $\varepsilon \sim 7.5$). This dielectric coverage, though as

thin as 10 μm, also alters the ideal antenna behavior and shifts down the resonance frequency.

The H-shaped antenna resembles the photoconductive antenna designs usually found in pulsed THz systems. It can be considered a dipole of the length L, with a correction of the effective dielectric constant calculated by the embedded or coated microstip formulas [33, 34]. Though there is no closed-form solution for the effective dielectric constant, it can be estimated as

$$\varepsilon_{eff} = \frac{\varepsilon_r + \varepsilon_0}{2} + \frac{\varepsilon_r - \varepsilon_0}{2\sqrt{\left(1 + 12\dfrac{H}{W}\right)}}$$

where H is the height of the dielectric, W is the width of the stripline (antenna wing), and ε_r is the dielectric constant of the passivation. The later value is estimated by the average value of the different layers that build up the passivation. In our cases, the passivation height between the antenna and the lower metal shields is approximately $H = 7$ μm, the width of the antenna wings is $W = 15$ μm, and $\varepsilon_r = 3.8$. The target frequency has been 360 GHz. The estimated antenna L_R size, using the half-wavelength dipole equation, becomes:

$$L_R = \frac{L_0}{\sqrt{\varepsilon_{eff}}} = \frac{\lambda_0}{2\sqrt{\varepsilon_{eff}}} \sim \frac{833\ \mu m}{2\sqrt{3.3}} = 228.5\ \mu m$$

Finally, the antenna has been drawn to $L = 230$ μm after EM simulation-based corrections. Figure 5.15 shows the simulated and measured response of this sensor, which show good correlation. The peak amplified responsivity is found to be 185 kV/W @ 365 GHz (1.85 kV/W unamplified responsivity) with open drain configuration and $V_{GS} = 0.2$V (see Figure 5.7). At the detectivity maximum ($V_{GS} = 0.36$V), though the responsivity drops to near half the above values, the NEP reaches $40\,pW/\sqrt{Hz}$.

5.7.3.2 Broadband Antenna

The case of the bow tie antennas is quite different and much more difficult to estimate by paper-and-pencil methods. Beneath the bow tie antennas there is no metal ground shield. Considering the dielectric around the antenna and the substrate with the metallic bottom plate of the packaging, this case can be more precisely modeled as a suspended microstrip structure with superstrate [34]. In order to find the physical dimensions for the resonance frequency, the effective relative permittivity must be derived first, which can be found in the literature as well [33]. In order to make better use of the silicon area, the four antenna detector pair is connected in series [14].

The difficulties arise from the substrate resonance, as the inevitable Fabry-Pérot interference will amend the ideal behavior. The typical wafer thickness of commercial CMOS technologies varies in between 200 and 300 μm. Taking into account the high refractive index of the silicon, this thickness is comparable to the wavelength of the sub-THz radiation in silicon. During hand calculations, the targeted frequency
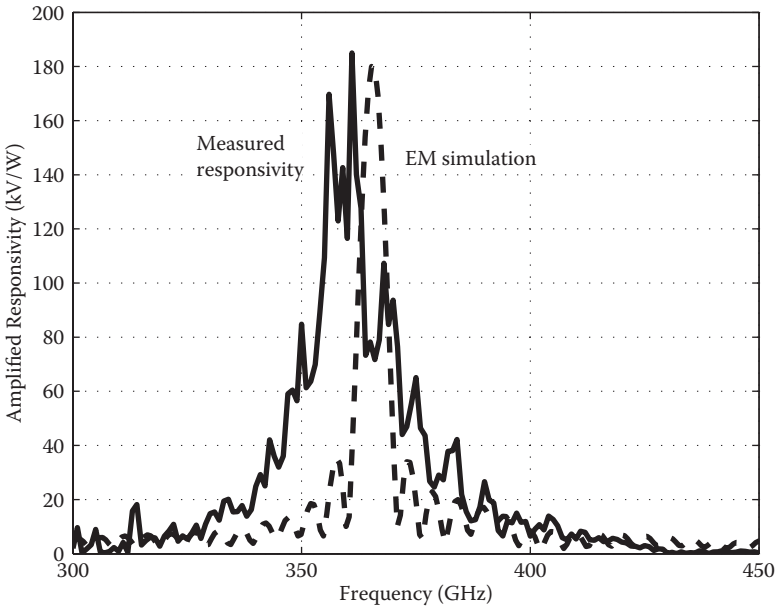
FIGURE 5.15   Simulated and measured responsivity of the H-shaped dipole antenna sensor.

has been the first significant water absorption peak at 550 GHz. Based on the substrate-air half-sphere model, the resonant size would be $L = 108$ µm. This peak is strongly shifted when the actual dielectric-substrate model and the very close other antennas are involved (Figure 5.16, top section). As a next step, the finite substrate is modeled. The substrate thickness at this technology is $H_{Si} = 270$ µm. This thickness with a metallic bottom plate would give minimum absorption (maximum antenna response) near 220, 380, 540, and 720 GHz and significant attenuation in between. Though the dielectric under the antenna and other metallic structures on the chip alter the simulated peaks, the resulting characteristic presented in the bottom section of Figure 5.7 clearly shows the measured effect of the substrate resonance. As a conclusion, the hand calculations did not conduct useful estimation compared to the successful former case, though detailed EM simulation helped to estimate the real behavior.

The sensor provides 52 kV/W amplified responsivity at 0.47 THz. At $V_{GS} = 0.2V$ the total thermal noise of the four detector is higher than the single detector, which results in $NEP \approx 540\, pW/\sqrt{Hz}$. The peak detectivity needs different settings, namely, $V_{GS} = 0.4V$ with 22 kV/W amplified responsivity and $NEP \approx 120\, pW/\sqrt{Hz}$.

5.8   APPLICATION EXAMPLES

5.8.1   Transmission Imaging

The first example is transmission imaging. The imaging setup (Figure 5.17) is based on reflective elements to allow broadband operation. High-resistivity
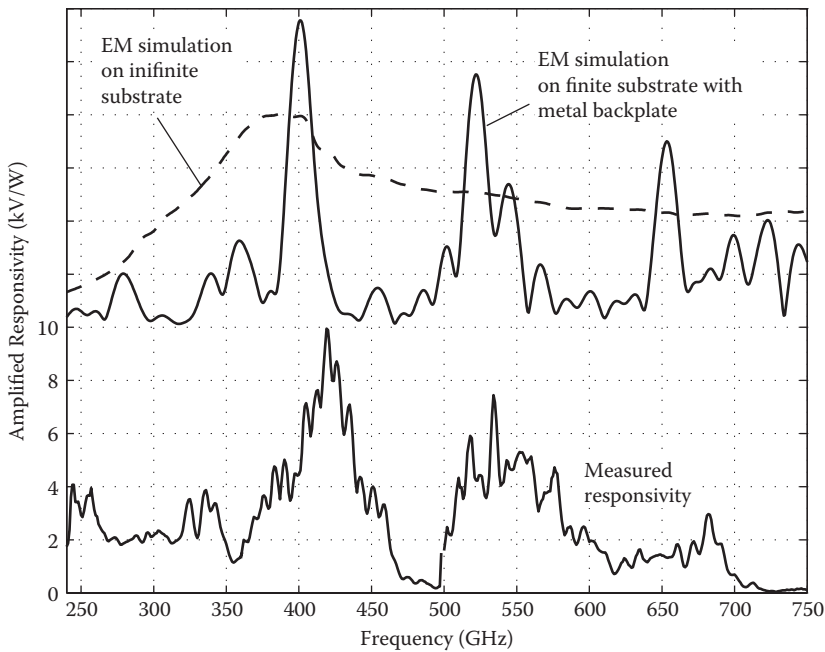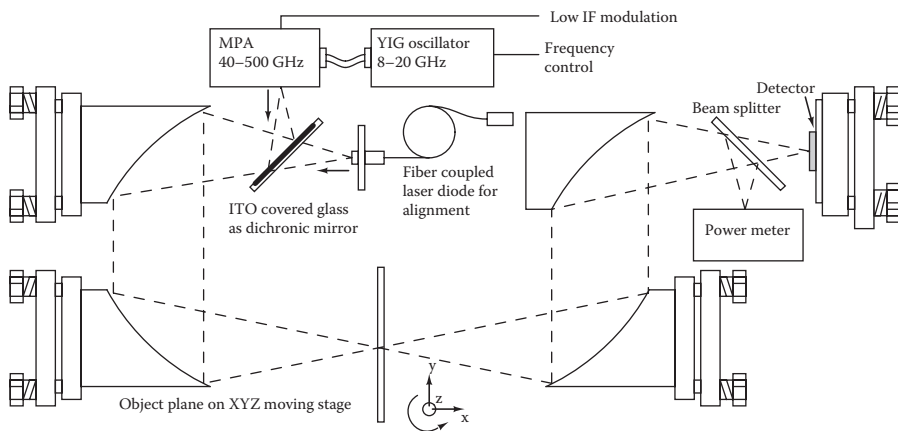
FIGURE 5.16   Simulated and measured responsivity of the four serially connected bow tie antenna sensors. The theoretical smooth and broadband response of the bow tie antenna is changed significantly due to the substrate resonance and the surrounding metal structures as shown in the upper part of the figure.

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FIGURE 5.17   Transmission image acquisition setup based on a CW sub-THz source and a quasi-optical arrangement. During the setup process, the high-resistivity silicon beam splitter is removed to aim positioning at the object plane.
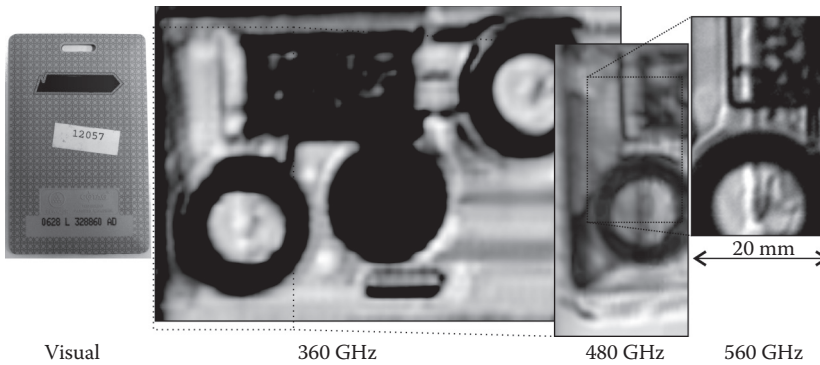
Visual   360 GHz   480 GHz   560 GHz

FIGURE 5.18 Transmission raster scan of an active RF entry card at different frequencies captured with different sensors.

floating zone silicon (HRFZ-Si) beam splitters are used. In order to aid the positioning, an ITO covered glass is placed as a dichroic mirror. During characterization, the absolute power meter is used, while during image acquisition its beam splitter is removed.

In the sample holder an entry card has been fixed, which is a battery-powered transmitter encapsulated into a plastic enclosure. At three wavelengths the entire and portions of the card have been raster scanned. The operation frequencies are selected as peaks of different antennas on the chip: at 360, 480, and 560 GHz the H-shaped, double-H-shaped, and bow tie antenna-coupled sensors were used, respectively. The scanning rasters were 0.5, 0.4, and 0.25 mm for the scans in both horizontal and vertical directions. The total scanned area was 80×55 mm at the lowest frequency, and smaller at higher frequencies. The pixel acquisition time varied from 20 to 1 Hz for different wavelengths in order to maintain the image signal-to-noise ratio (SNR), as the corresponding resonant antennas have different sensitivities. The visual and the scans can be seen in Figure 5.18.

5.8.2 COMPLEX WAVEFORM DETECTION

As an application example, a homodyne mixing setup and results are presented. The FET detectors are capable of homodyne or heterodyne mixing according to [12, 13]. These modes help to improve the acquisition SNR. The homodyne detection is based on the self-interference of a coherent wave, which in our case is provided by the electronic multiplier-based source. The source wave is divided into an object and a reference beam, and their interference is captured on the chip surface. The common problem with homodyne imaging is that the interference pattern contains information of the phase difference and the intensity of the object, but this information cannot be separated by a single recording. A usual solution is applying the mechanical delay stage to sweep the reference at least a wavelength to capture phase relations and derive intensity value. This method is inherently slow.

A single-shot quadrature phase-shifting interferometry architecture is presented in [32] that is capable of recording multiple phase-shifted interference values without mechanical translation. The method is based on orthogonally polarized object and reference beams and on linear and circular polarization-sensitive antennas in space-division multiplexing. The method handles the FETs as a square law detector, the response of which depends on the drain-source and gate-source RF voltage. In mixing, the FET's response is approximated as [5]

$$V_R \cong \eta \frac{-\left(U_{DS}^{THz}\right)^2 - \left(U_{DS}^{THz}\right)^2 + 2\left(U_{DS}^{THz} U_{DS}^{THz}\right)\cos\varphi}{4(U_{GS} - U_{DS})}$$

where ϕ is the phase difference between the two incident coherent waves and the two waves are coupled independently to the gate-source and drain-source terminals. In our circuit, there is only a gate-source connection $\left(U_{GS}^{THz} = 0\right)$ and the antenna provides the wave superposition; hence, the above equation becomes simpler. The simplified equation is equal to the square power detection model:

$$V_R \cong \eta \frac{-\left(U_{GS}^{THz}\right)^2}{4U_{GS}}$$

This gate-source voltage was transformed from the free space waves by the antennas through their antenna resistance. By substituting the incoming object and reference wave powers (P_O, P_R), the antenna resistance (R_A), and the phase difference (ϕ), one can get a similar equation for a linear polarization antenna:

$$V_{R, linear} \cong \eta \frac{-R_A P_O - R_A P_R \pm 2R_A \sqrt{P_O P_R}\,\cos\varphi}{4U_{GS}}\alpha \pm \cos\varphi$$

where the antenna polarization lies in between the orthogonally polarized beams, as can be seen in Figure 5.19. The circular polarization antenna-coupled detector's
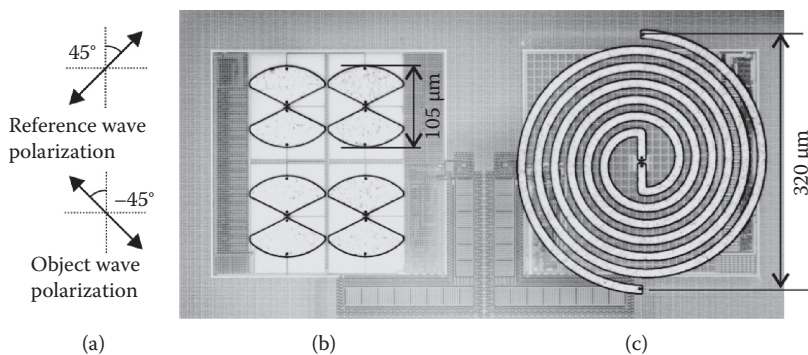

45°

Reference wave
polarization

−45°

Object wave
polarization

105 µm

320 µm

(a)   (b)   (c)

FIGURE 5.19   Microphoto of the bow tie and spiral antenna sensors and the incident reference and object beam polarization.

response will differ from this value, because the circular wings introduce a phase shift in one of the beams coupling to the detector. The sign of the dependence flips using left-handed or right-handed circular polarization:

$$V_{R,circular} \cong \eta \frac{-R_A P_O - R_A P_R \pm 2R_A \sqrt{P_O P_R} \sin \varphi}{4U_{GS}} \alpha \pm \sin \varphi$$

Hence, one can measure two beams independently (i.e., the object and reference beams) and acquire quadrature interferences of 0, $\pi/2$, π, and $3\pi/2$ radians by selecting, aligning, and rotating the linear and changing the handedness of circular polarized antenna-coupled detectors.

In the experiment two antennas are selected, a bow tie and an Archimedean spiral, as linear and circular polarized types, respectively. In the optical setup, the reference beam is separated and wire grid polarizers are included as well. The setup is shown in Figure 5.20.

In the presented example a PMMS lens has been raster scanned and at each point at 360 GHz. The complex amplitude is recorded as in-phase and quadrature phase interference patterns. The reconstruction of the intensities and phase is straightforward from these data. The exact dimensions of the lens are diameter of 38 mm, focal length of 65 mm @ 360 GHz, and physical thicknesses at the perimeter and center of 2.3 ± 0.05 and 6.5 ± 0.05 mm, respectively. The refractive index of the lens was $n = 1.57 \pm 0.05$ @ 360 GHz. The lens has been placed in the translation stage and the interferograms are recorded in a 30 by 30 mm area with 0.5 mm step size. After reconstructing the intensity and phase, the phase image is unwrapped using a standard method [39]. The measurement steps are shown in Figure 5.21.

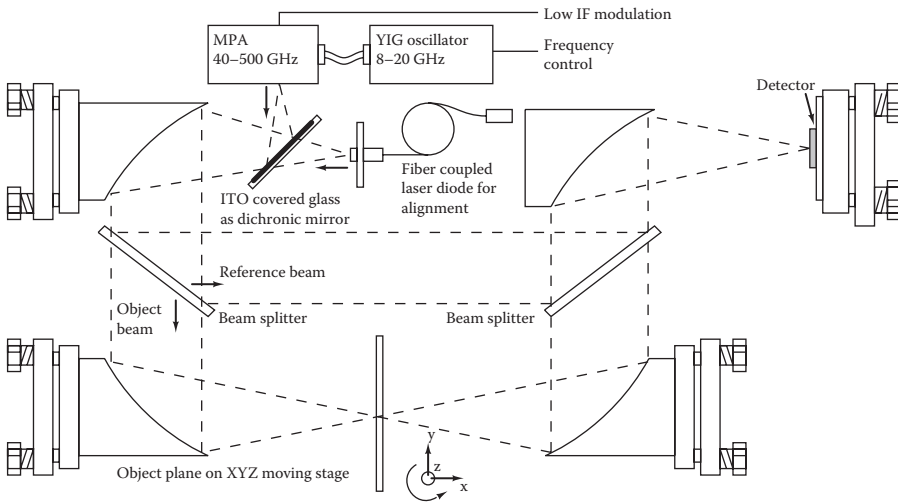AU: Please spell out PMMS for first use.

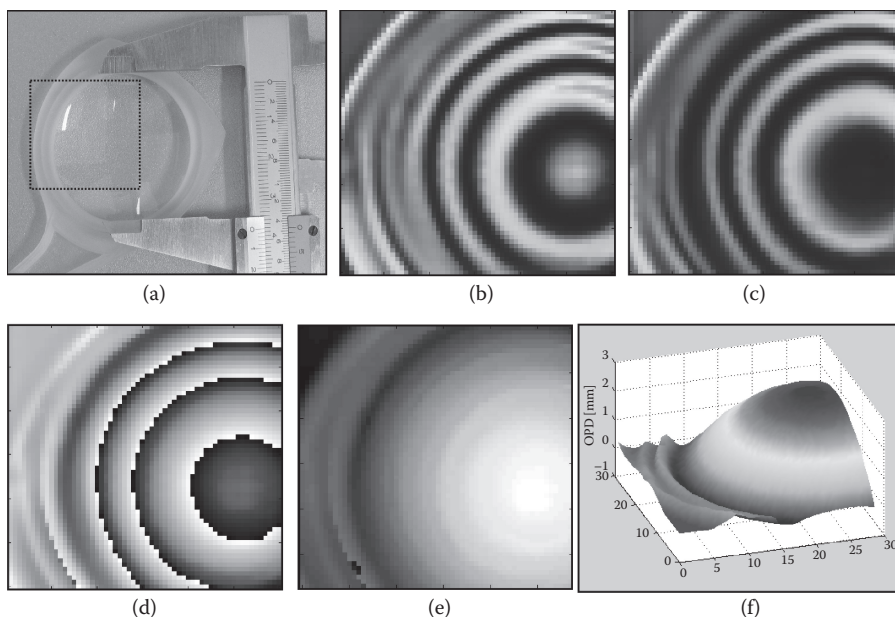**FIGURE 5.20**   Homodyne interference image acquisition setup.

FIGURE 5.21   (a) Photograph of the lens with the raster scanned area of 30 by 30 mm. (b) In-phase interferogram captured by the linear antenna detector. (c) Quadrature interferogram captured by the circular polarization antenna detector. (d) Reconstructed phase image. (e) Unwrapped phase image. (f) Pseudoview of the estimated optical path delay.

5.9   CONCLUSIONS

It has been shown how a versatile imaging system has been integrated around the very same detector. The resulting system autonomously tracks an externally modulated signal and finally provides a compact digital stream containing the measured intensity values of the selected sensors. The practical examples showed that instead of placing an array of identical sensors within the diffraction-limited spot, the integration of different antenna structures yields more interesting and useful applications: broadband response from 0.25–0.7 THz with different polarization sensitivities.

ACKNOWLEDGMENTS

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