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Formation and Thermoelectric Properties of Si/$CrSi_2$/Si(001) Heterostructures with Stressed Chromium Disilicide Nanocrystallites

Dmitry Goroshko,[1,2,*] Evgeniy Chusovitin,[1] Dmitry Bezbabniy,[3] Laszlo Dózsa,[4] Bela Pécz,[4] and Nikolay Galkin[1,2]

[1]Institute of Automation and Control Processes of Far Eastern Branch of Russian Academy of Sciences, Vladivostok 690041, Russia
[2]Far Eastern Federal University, Vladivostok 690950, Russia
[3]Amur State University, Blagoveschensk 675027, Russia
[4]Research Institute for Technical Physics and Materials Science, Budapest H-1525, Hungary

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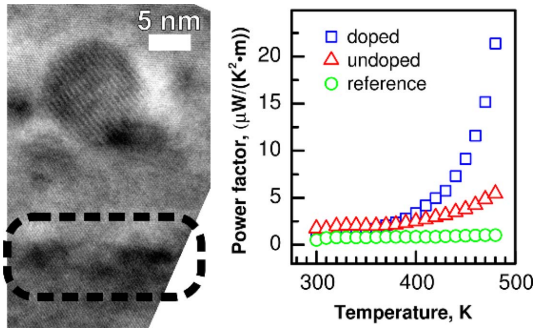
Three-layer heterostructures with embedded $CrSi_2$ nanocrystallites were grown using molecular-beam epitaxy. The nanocrystallites have epitaxial orientation to the silicon lattice and are subjected to anisotropic compressive stress in the $CrSi_2$ [001] direction. The thermoelectric power factor of the heterostructure is about 5 times higher than that in the substrate at 300 - 480 K. Taking into consideration the ratio of nanocomposite and substrate thickness, the real power factor is expected to be 2 - 3 orders higher than the measured one and it reaches 3200 μW K^{-2} m^{-1} at 470 K.

Keywords: nanocomposite, self-organization, thermoelectric materials, compound semiconductors, heterostructures



1. INTRODUCTION

Compounds of transition metals with silicon have many interesting applications in microelectronics because they have favorable physical properties, and their formation conditions are suitable for conventional silicon processing. Chromium disilicide ($CrSi_2$) has attracted much attention because it has a narrow bandgap, E_g = 0.35 eV,[1] and good thermoelectric properties at high temperatures.[2] Moreover, $CrSi_2$ has the smallest mismatch with the silicon lattice compared to other transition metal silicides.[3] The epitaxial growth of $CrSi_2$ in the form of islands and thin films has already been studied on Si(111) substrates.[4] Formation of a nanocomposite based on silicon and silicides has great potential for technological usage. It was shown[5] that the thermoelectric power of the Cr_xSi_{1-x} nanocomposite depends on the crystallization degree and the *ZT* is at least two times higher than that for bulk $CrSi_2$. This could be explained by the rearrangement of the electronic structure of chromium silicide precipitates because of internal stress. The stress appears because of the lattice mismatch of the contacting materials and deformation of the crystal lattice. It was theoretically shown[6] that 6% uniaxial tensile stress of the lattice turns $CrSi_2$ to a direct-gap semiconductor with a bandgap of about 0.3 eV. Formation of $CrSi_2$ in the form of high density arrays of nanocrystallites (NCs) embedded into the monocrystalline silicon makes it possible to precisely control the stress developed in the silicide and achieve high values of thermoelectric efficiency. The latter could be obtained through confinement of thermal conductivity in an inhomogeneous medium.[7] Previously, we developed a method of fabrication of $CrSi_2$ nanocomposites on Si(111) substrates.[8] However, from the technological point of view, (001) silicon surface orientation is more preferable. This study is devoted to the investigation of the formation and thermoelectric properties of chromium disilicide-based nanocomposites on Si(001). We will show that over the temperature range of 300 to 480 K, the thermoelectric power factor of Si/$CrSi_2$-NC/Si(001) heterostructure is about 5 times higher than that in the substrate.

*Corresponding author: goroshko@iacp.dvo.ru
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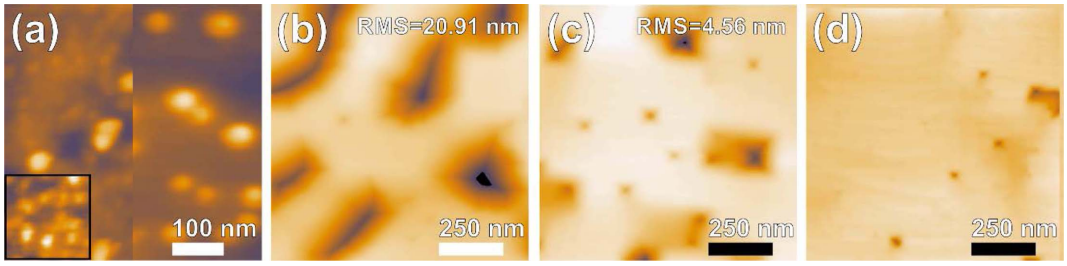

Fig. 1. (a) AFM image of silicon surface with NCs of $CrSi_2$ grown using reactive deposition (left) or solid phase (right) epitaxy of a 0.4 nm-thick Cr layer. An inset in the figure shows the presence of a high-density array of NCs with small size. (b), (c) AFM images of the 230 nm silicon capping layer deposited over the chromium silicide nanocrystallites at 670°C and 600°C. (d) AFM image of the heterostructures with three layers of $CrSi_2$ NCs separated by epitaxial silicon layers (230 nm). Chromium disilicide was formed by SPE of a 0.2 nm-thick Cr layer.

2. EXPERIMENTAL PROCEDURE

The details of the substrate preparation and growth procedure are described elsewhere.[8] Chromium disilicide nanocrystallites were grown using two methods. The first one is a reactive deposition epitaxy (RDE) of 0.2 - 0.4 nm chromium on Si(001) substrate heated up to 500°C. The second is solid phase epitaxy (SPE) of the same amount of Cr on the substrate kept at room temperature followed by annealing at 550°C for 20 min. In both cases, a high-density array of $CrSi_2$ NCs was obtained. A silicon layer of thickness 100 - 230 nm was deposited on the substrate with $CrSi_2$ NCs at 550 - 700°C. During the overgrowth process, the almost flat silicide nanocrystallites transform into spherical nanocrystallites. By repetition of the Cr deposition and silicon layer overgrowth, three-layer heterostructures were grown. Since the *ZT* value is directly proportional to the sample conductivity, a high concentration of majority carriers is required. It is known[9] that Al atoms are *p*-type dopants for both silicon and $CrSi_2$. Before the formation of chromium disilicide, a thin layer (about 0.05 nm) of Al was deposited at RT on the substrate with the aim of forming a doped nanocomposite. Thermoelectric properties of the samples were measured using a homemade setup, which consists of a vacuum chamber, main furnace, two gradient furnaces, two gradient thermocouples, and voltmeters. Non-rectifying electrical contacts were fabricated by ultrasonic soldering of 20 μm Al wires to the bonding pads on the film side. The pads were prepared by mask deposition of 1 μm Al followed by 10 min annealing at 450°C. The distance between the contacts was 7 mm. All the measurements were carried out along the sample plane over the temperature range 300 - 480 K.

3. RESULTS AND DISCUSSION

Figure 1(a) shows the atomic-force microscopy (AFM) images of the substrates with NCs of chromium disilicide formed using RDE and SPE techniques. The main difference between the RDE and SPE NCs growth methods is the density and the sizes of the grown nanocrystallites. RDE results in the formation of NCs of two types with different heights (2 and 8 nm). Nanocrystallite surface concentration was about 2×10^{11} and 2×10^{9} cm^{-2} for the small and big NCs, respectively (Fig. 1(a), left region). In the case of SPE, NCs of intermediate size are observed with a concentration of 1×10^{10} cm^{-2} (Fig. 1(a), right region).

Formation of the small NCs with high density using reactive deposition epitaxy can be explained by limited surface diffusion of chromium atoms. The big islands, with a density two orders of magnitude lower than the small islands, are the result of the coalescence of small NCs. In the case of SPE, during annealing for 20 min the small NCs move on the surface and coalesce. It results in a NCs array formation with intermediate size and concentration of NCs.

Previously, it was shown that 100 nm silicon deposited at 750°C is enough for complete embedding of $CrSi_2$ NCs grown by reactive epitaxy of 1.5 nm Cr on the Si(111) substrate, and for the formation of smooth and flat silicon surfaces.[8] However, in the case of Si(001) substrate, these growth parameters were not appropriate for defect-free surface formation. AFM data showed that only 230 nm of silicon is sufficient to get smooth and flat surfaces. To study how the surface quality of the capping layer depends on the growth temperature, we created a temperature gradient along the substrate with NCs: the coldest side was at 600°C and the hottest was at 670°C. According to AFM data, the temperature gradient leads to a 5-fold increase in the surface root-mean-square roughness (RMS) on the hot side (Fig. 1b and c). Thus, for formation of a silicon capping layer in multilayer heterostructures, we chose a layer thickness of 230 nm and growth temperature of 600°C.

Figure 1(d) shows the surfaces of the three-layer heterostructure with NCs grown using SPE. As a reference, we used a sample with three silicon epitaxial layers grown on the clean Si(001) substrate, but without $CrSi_2$ NCs. The reference sample has the smoothest surface with a roughness of 0.26 nm. Roughness of the samples with NCs was higher

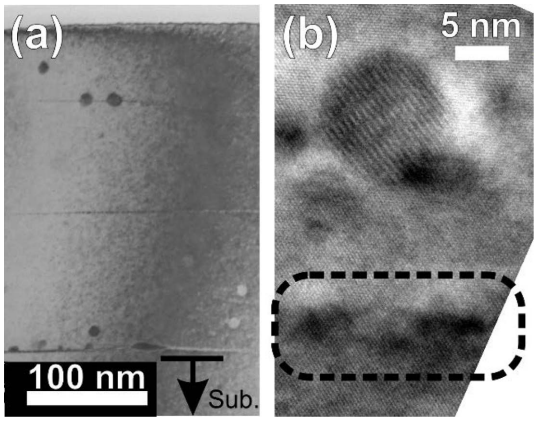

Fig. 2. (a) TEM bright-field image of the cross section of the three-layer heterostructure with $CrSi_2$ NCs formed by SPE of 0.2 nm Cr followed by 20 min annealing at 550°C. Nominal thickness of the separation layers is 230 nm. (b) HRTEM image of chromium disilicide nanocrystallite located near the deposition depth. There is an array of small NCs marked with the dashed line in the bottom part of the figure. Such arrays are visible as borders between layers in (a).

but did not exceed 1.5 nm. In all the cases, the capping layers were epitaxial, which was confirmed by the bright 2 × 1 low energy electron diffraction pattern with low background intensity. Three-layer heterostructures and the reference sample have small pits with identical concentrations of about 5×10^8 cm^{-2}. The lateral size of the pits is 5 - 30 nm and depth about 10 nm. The pits do not originate from the fully coalesced silicon blocks. It is worth noting that the third cap layer quality is sufficient to form another layer of the heterostructure. Thus, by repeating the procedure of $CrSi_2$ NCs formation followed by silicon overgrowth, one can make as many layers of the embedded nanocrystallites as required for the formation of appropriate thickness of the active region in the heterostructure.

The three-layer heterostructure with $CrSi_2$ NCs formed by SPE was investigated using transmission electron microscopy (TEM) and TEM with high resolution (HRTEM). In Fig. 2(a), three silicon layers divided by sharp borders are clearly seen. These borders correspond to the surfaces where the formation of $CrSi_2$ NCs took place. In addition, one can see some large crystallites of a spherical shape (Fig. 2(a)). A magnified image of such nanocrystallites is shown in Fig. 2(b). Comparison of the size and the concentration of NCs obtained from the TEM image with that calculated from the AFM data indicates that the flat uncovered NCs and the spherical NCs found in the cross-sectional TEM image of the epitaxial layers are the same $CrSi_2$ particles.

It is difficult to determine the structure of $CrSi_2$ NCs by x-ray or micro-diffraction because of the small quantity of the silicide phase. In this work, the structure of $CrSi_2$ was determined by Fourier transformation (not shown). It was determined that the $CrSi_2$ NC has the following epitaxial orientation with the silicon lattice: $CrSi_2(001)||Si(111)$ with $CrSi_2[010]||Si[110]$. The period of $CrSi_2$ atomic planes in the [001] direction is 0.6173 nm, while in the bulk $CrSi_2$ crystal, it is 0.6374 nm.[10] The mismatch in the $CrSi_2$[001] direction is about 3.2%, resulting in an anisotropic compressive stress of the nanocrystallite. Nevertheless, nanocrystallites have a sharp heterojunction with silicon and reveal defect-free incorporation into the lattice.

Some of the nanocrystallites are stabilized at the deposition depth while others are located inside epitaxial layers. This result corresponds to the formation of $CrSi_2$ NCs on the Si(111).[11] The effect of "floating" of NCs consisting in the moving of nanocrystallites from the deposition depth is obvious (Fig. 2(a)). The reason of this phenomenon could be the shifting of the $CrSi_2$ NCs on the silicon surface during Si overgrowth by the silicon step bunches.[12] When moving nanocrystallites come across a defect on the silicon surface, they could adhere to the surface and silicon begins to cover them. Hence, in the cross-sectional TEM image this NC seems to be "floating". In some cases, the NCs could "float" through the entire capping layer and emerge just beneath the surface. In this case, we can observe small pits located over such NCs.

Let us consider the structure of the boundaries of the epitaxial silicon layers. Figure 2(b) shows that the high contrast of the borders is due to the presence of individual nanocrystallites with size 1 - 2 nm. The TEM image resolution is not sufficient to determine the object structure, but taking into account the fact that they occur in the $CrSi_2$ formation area, one can suggest that they consist of only $CrSi_2$. In the AFM image, such very small nanocrystallites are not visible because the resolution limit of the standard cantilever that was used for AFM measurements is about 10 nm, which is insufficient to distinguish objects with a lateral size of 1 - 2 nm. It is possible that the substrate surface between the $CrSi_2$ NCs (Fig. 1a, right part) is filled with a high-density array of the small $CrSi_2$ NCs, which appears as the sharp border in the TEM image (Fig. 2a). The small NC array on the sample surface could be the reason for the difficulties in the cap silicon layer growth.

Measurements of the electrical properties of doped and undoped three-layer heterostructures with embedded $CrSi_2$ NCs along with the reference sample were carried out over the temperature range 300 - 480 K. The Hall voltage in all the cases has a positive sign, indicating the conservation of *p*-type conductivity in the three-layer heterostructure.

It was observed that embedding of the NCs reduces the majority carrier mobility (Fig. 3(a)), which is associated with an increase of the carrier scattering on the NCs. At the same time, difference in the mobility in the doped and undoped heterostructures is insignificant. At a temperature of 470 K, the hole concentration increase in the undoped heterostructure was 6 times while in the doped heterostructure it was 20

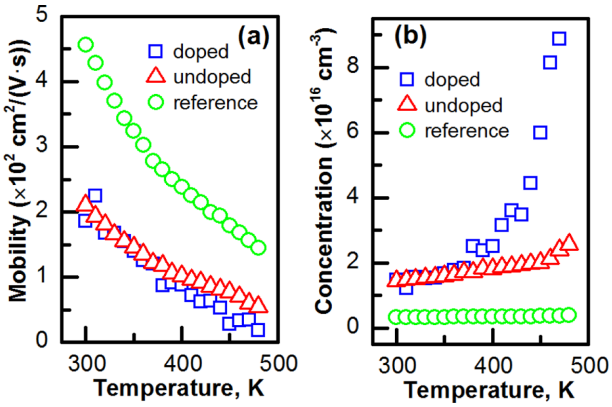

Fig. 3. Dependence of hole mobility (a) and concentration (b) on temperature for the reference sample and for three-layer doped/undoped heterostructures with embedded $CrSi_2$ NCs.

times, relative to the reference sample. At room temperature, an increase in the hole concentration in the doped and undoped sample is the same, about 4 times, which is due to the emission of carriers from the narrow-gap chromium disilicide into silicon (Fig. 3(b)). The temperature growth results in a sharp increase in the hole concentration in the doped heterostructure because of the activation of the aluminum acceptor levels (in silicon $E_a = 67$ meV[9]). The majority carriers increase, despite the mobility decrease, leading to an increase in the conductivity by 2 - 2.5 times for the undoped heterostructure over the temperature range 300 - 470 K and by 6 times for the doped heterostructure at 470 K (Fig. 4(a)).

It should be noted that the Seebeck coefficient obtained for the doped sample over the temperature range 370 - 470 K is higher than for the undoped sample, which is unusual for conventional thermoelectric compounds. We suppose that doping of our heterostructure results in the formation of an impurity band within the $CrSi_2$ NCs bandgap. The impurity band leads to an abrupt change in the density of states. Since the thermopower is a measure of the asymmetry in electronic structure near the Fermi level,[13] the Seebeck coefficient in the doped sample will begin to increase when the Fermi level reaches the impurity band. A similar result was reported[14] during the doping of PbTe with Tl: despite the significant carrier concentration growth, there was no decrease in thermopower. In our case, the Fermi level of a doped sample reaches the impurity band at a temperature of about 370 K; after this point, the Seebeck coefficient of the doped sample increases faster than that of the undoped sample.

Using the conductivity and Seebeck coefficient data (Fig. 4(a), (b)), the power factor = $\alpha^2 \times \sigma$ was calculated, where α is the Seebeck coefficient and σ is the electrical conductivity. It was observed that the power factor (PF) of an undoped three-layer heterostructure at 470 K is five times greater than

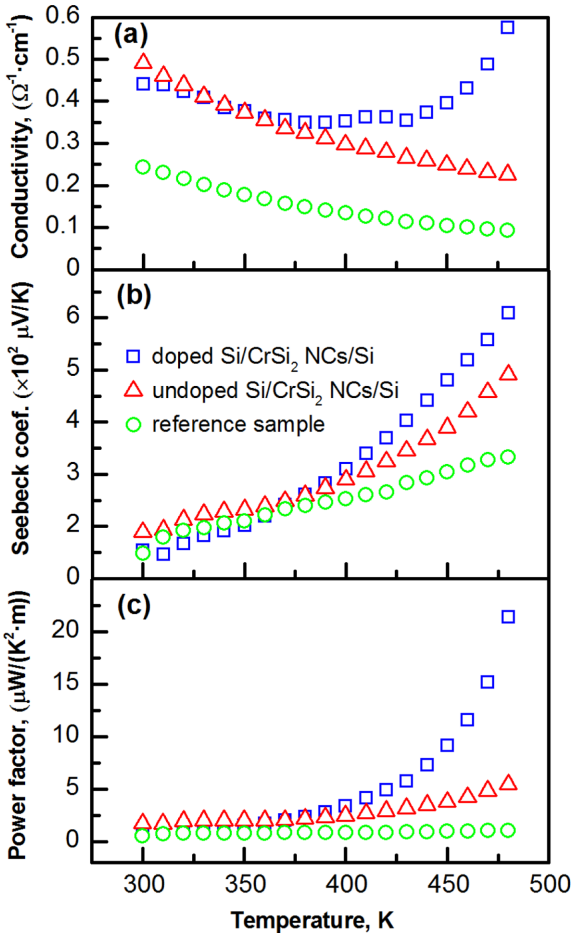

Fig. 4. Temperature dependence of conductivity (a) Seebeck coefficient (b), and power factor (c) for reference sample and for the three-layer heterostructure with embedded $CrSi_2$ NC grown by SPE, with and without doping.

the power factor of the reference sample; for a doped heterostructure, this difference in power factor is even higher, 20 times. Such a large difference occurs because of the charge carrier thermal emission from NCs and because of the increase in conductivity at the expense of doping. Compared to the data reported by Schumann *et al.*,[5] who investigated bulk samples of silicon nanocomposites with $CrSi_2$ precipitates, the Seebeck coefficient value of our heterostructure is the same at a temperature 300 K, but it is 2 - 3 times higher at 470 K. However, the power factor of our heterostructure is lower by more than two orders of magnitude. This fact can be explained by the significant substrate contribution. Calculations of the majority carrier concentration, carrier mobility, and conductivity presented in Fig. 3 and 4(a) have been done for the heterostructure within the framework of a bulk model.[9] The calculated values are effective; they involve two contributions: from the substrate and from the epitaxial layers with embedded $CrSi_2$ NCs. Given that the thickness of the epitaxial layer is approximately

350 nm and the substrate thickness is 350 μm, which is three orders of magnitude greater than the thickness of the film, one can assume that the conductivity of the epitaxial layers with embedded NCs should be considerably greater than the calculated value. As a first approach, we can consider our system as two conducting layers (film and substrate) connected in parallel; then the relationship between the effective (measured) conductivity and the conductivity of each layer will be described by equation:[15]

$$\sigma_{eff.}(d_{sub.}+d_{film}) = \sigma_{sub.}d_{sub.} + \sigma_{film}d_{film}$$

where $\sigma_{eff.}$ is the effective value of sample conductivity, σ_{sub} and σ_{film} are part of conductivity that is related to the substrate and epitaxial film with NCs, respectively; $d_{sub.}$ and d_{film} are the thickness of silicon substrate and epitaxial layers with NCs. Using the values of conductivity from Fig. 4(a) at room temperature and 470 K, we calculated σ_{film} and substituted it to the equation for the power factor. The Seebeck coefficient for the calculations was obtained from Fig. 4(c). Based on these assumptions, we estimated the power factor for undoped and doped films with NCs.

For undoped heterostructures, the PF is equal to 880 and 3200 μW K^{-2} m^{-1} at 300 and 470 K, respectively. In the case of the doped heterostructure, the PF value at 470 K is higher by almost an order of magnitude. The obtained PF value exceeded all the published data on the thermoelectric parameters of nanodispersed chromium disilicide films,[5] and of nanostructured bulk $Si_{0.8}Ge_{0.2}$ alloys with embedded $CrSi_2$.[16]

4. CONCLUSIONS

In this study, it was shown that it is possible to form multilayer silicon heterostructures with buried $CrSi_2$ nanocrystallites on the Si(001) substrate, with as many layers as desired. The embedded $CrSi_2$ NCs could be formed using both RDE and SPE of thin chromium layers (0.2 - 0.4 nm) followed by silicon overgrowth. It has been found that near optimal conditions for the growth of flat and smooth cap silicon layer on Si(001) is molecular beam epitaxy of 230 nm silicon at 600°C. This results in the full embedding of $CrSi_2$ NCs formed using RDE or SPE of 0.2 nm of Cr.

According to the cross-sectional TEM images of the three-layer heterostructure, the embedded $CrSi_2$ NCs formed by SPE has a spherical shape with a diameter of 12 ± 2 nm. They are epitaxially oriented in the silicon: $CrSi_2(001)||Si(111)$ with $CrSi_2[010]||Si[110]$. They have anisotropic compressive stress in $CrSi_2[001]$ direction of about 3.2%. From the TEM data, it was observed that some of the nanocrystallites have a tendency to "float" towards the surface, while others stay at the deposition depth. It is proposed that this phenomenon is due to the migration of $CrSi_2$ NCs on the surface during silicon overgrowth. A five-fold increase of the effective power factor at 480 K was observed for the three-layer heterostructure, compared to a clean silicon substrate. Given that the substrate thickness is 3 orders of magnitude higher than the total thickness of the grown silicon layer with embedded NCs, one can assume that the actual value of the thermoelectric efficiency of the nanocomposite layer should be 4 orders of magnitude higher than the measured value for the doped sample.

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REFERENCES

1. V. E. Borisenko, *Semiconducting Silicides*, p. 192, Springer, Berlin, German (2000).
2. T. Ohkoshi, Y. Isoda, H. Kaibe, S. Ichida, K. Matsumoto, and I. Nishida, *T. Jpn. I. Met*. **29**, 756 (1988).
3. O. Filonenko, M. Falke, H. Hortenbach, A. Henning, G. Beddies, and H.-J. Hinneberg, *Appl. Surf. Sci*. **227**, 341 (2004).
4. N. G. Galkin, T. V. Velitchko, S. V. Skripka, and A. V. Khrustalev, *Thin Solid Films* **280**, 211 (1996).
5. J. Schumann, C. Gladun, J.-I. Monch, A. Heinrich, J. Thomas, and W. Pitschke, *Thin Solid Films* **246**, 24 (1994).
6. A. V. Krivosheeva, V. L. Shaposhnikov, and V. E. Borisenko, *Mater. Sci. Eng. B-Adv.* **101**, 309 (2003).
7. A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard III, and J. R. Heath, *Nature* **451**, 168 (2008).
8. N. G. Galkin, D. L. Goroshko, S. A. Dotsenko, and T. V. Turchin, *J. Nanosci. Nanotechno.* **8**, 557 (2008).
9. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, pp. 23-30, Third Ed., Wiley-Interscience, Hoboken, New Jersey, USA (2007).
10. JCPDS File Card No. 81-0166.
11. N. G. Galkin, L. Dózsa, E. A. Chusovitin, B. Pécz, and L. Dobos, *Appl. Surf. Sci*. **256**, 7331 (2010).
12. A. V. Latyshev, L. V. Litvin, and A. L. Aseev, *Appl. Surf. Sci.* **130-132**, 139 (1998).
13. B. A. Akimov, A. V. Dmitriev, D. R. Khokhlov, and L. I. Ryabova, *Phys. Status Solidi A* **137**, 9 (1993).
14. J. P. Heremans, V. Jovovic, E. S. Toberer, A. Saramat, K. Kurosaki, A. Charoenphakdee, Sh. Yamanaka, and G. J. Snyder, *Science* **321**, 554 (2008).
15. R. L. Petritz, *Phys. Rev.* **110**, 1254 (1958).
16. Z. Zamanipour and D. Vashaee, *J. Appl. Phys*. **112**, 093714 (2012).