

# Contact Problems in GaAs-based Solar Cells

**Antal Ürmös<sup>1</sup>, Zoltán Farkas<sup>1</sup>, László Dobos<sup>2</sup>, Szilvia Nagy<sup>3</sup>,  
Ákos Nemcsics<sup>1,2</sup>**

<sup>1</sup> Institute of Microelectronics and Technology, Óbuda University, Tavaszmező utca 17, H-1084 Budapest, Hungary

<sup>2</sup> Centre for Energy Research, Institute of Technical Physics and Materials Science, Konkoly Thege M. út 29-33, H-1121 Budapest, Hungary

<sup>3</sup> Department of Infocommunications, Széchenyi István University, Egyetem tér 1, H-9026 Győr, Hungary

e-mail: urmos.antal@kvk.uni-obuda.hu, farkas.zoltan@kvk.uni-obuda.hu,  
nagysz@sze.hu, nemcsics.akos@kvk.uni-obuda.hu

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*Abstract: The present work deals with contact problems of GaAs-based solar cells. In the introduction the most basic GaAs-based solar cell structures are introduced. Then, the energy and electronic properties are investigated. In the third part of this publication, the technological aspects of the metallization are discussed. Here the surface patterns are investigated, that are formed at the surface of the Au/GaAs and Au/TiN/GaAs material systems, as the effect of the annealing process. The further aim of these investigations to investigate, how the properties of ohmic contact depends on the properties of the material system. If these relations are known, the relationships between different morphologies and their electric qualities will be also known.*

*Keywords: solar cell; ohmic contacts; surface pattern; fractal dimension; structural entropy*

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## 1 Introduction

It is a well known fact that almost all of our energy sources originate with solar radiation, which is a renewable energy. One possible tool to directly utilize solar radiation, is the solar cell. The efficiency of solar cells is strongly influenced by the material band structure of the semiconductor. According to calculations, the optimal band gap is 1.4 eV. Such a material is, for example, GaAs. The efficiency of different solar cell structures may diverge from the theoretical calculations [1] in reality due to losses (thermal, reflection, recombination, etc) or due to cell construction issues (tandem, multiband solar cell, etc) [2].

This efficiency barrier can be surpassed with multiband devices. A limit of such methods of efficiency improvement is the finite number of the different semiconductors that can be integrated in a single solar cell. This newer barrier, in turn, can be surpassed by using multiple heterojunction or nanostructure type GaAs based solar cells. These devices utilize a wider wavelength interval of the solar spectrum.

Solar cells with single heterojunction GaAs-based structures are grown with metal-organic vapor phase deposition, and these solar cells are produced with lithography, heat treating and dry etching technology. The structures of these cells are shown in Fig. 1. The heterojunction is formed on a n-GaAs substrate. First, a buffer layer is grown on the substrate, and then a back surface field is formed. The base and emitter are formed on this layer then a window layer is deposited. The forward contact is a Ti/Pt/Au layer; the hind contact is an AuGe/Ni/Au layer.

<b>Front contact (Ti/Pt/Au)</b>	<b>500 nm</b>
<b>Ohmic p-GaAs</b>	<b>300 nm</b>
<b>Window p-In<sub>0.5</sub>Ga<sub>0.5</sub>P</b>	<b>200 nm</b>
<b>Emitter p-GaAs</b>	<b>500 nm</b>
<b>Base n-GaAs</b>	<b>3500 nm</b>
<b>BSF n-In<sub>0.5</sub>Ga<sub>0.5</sub>P</b>	<b>50 nm</b>
<b>Buffer n-GaAs</b>	<b>200 nm</b>
<b>Substrate n-GaAs</b>	<b>350 μm</b>
<b>Back contact (AuGe/Ni/Au)</b>	<b>500 nm</b>

Figure 1

Structure of a single heterojunction GaAs solar cell (source: [3])

There are other possible structures as well. Such a possibility is GaAs thin layer on a flexible substrate [4] or a sandwich structure of GaAs-Ge layers [5]. The goal regarding the latter structure was to increase the output current with Ge which has almost identical lattice constant than that of GaAs (Fig. 2). The 3 μm thick GaAs layer absorbs the greater proportion of the spectrum of Sun. The other parts of the spectrum is absorbed by Ge layer between 0.9 μm and 108 μm. The greater part of the spectrum is absorbed by the first 500 nm of the 5 μm thick Ge layer. The charge carriers that were generated in Ge drift to the GaAs layer and they are added to the charge carriers generated there. The quality of Ge and GaAs layers causes longer majority charge carrier lifetime thus the output current increases.

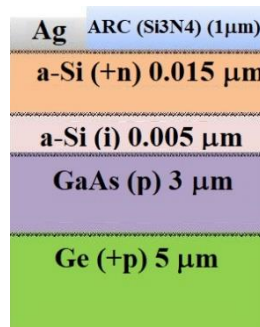


Figure 2

Structure of a single heterojunction "sandwich" GaAs-Ge solar cell (source: [3])

Multiple heterojunction GaP/GaAs/Ge multiple bands solar cells are grown by metal-organic chemical vapor phase deposition or by molecular beam epitaxy. Multiple junction solar cells consist of single junction solar cells stacked onto each other. The structure of the multiple junction solar cells is such that the band gap of each layer is thinner than that of the previous ones. The efficiency of these solar cells can be as high as 32%.

The group called nanostructure solar cells, is a special subgroup of the multiple junction solar cells [4] [5] [6]. In the case of this special subgroup, multiple quantum dot layers can be found in the band gap. These devices are referred to as IBQD - Intermediate Band Quantum Dot Sc. Numerous authors have already published papers on these structures [7] [8] [9] [10] [11]. These quantum dot layers are "inserted" between the usual p and n layers.

## 2 Electrical Aspects of the Contact

### 2.1 Energy Structure at the Contact Function

The contacts are vital parts of the GaAs based solar cells, since the device communicates with the environment through contacts. The III-V based compound semiconductors have several contact systems. The quality of these semiconductor systems play a key importance regarding the operation of solar cells and other electronic devices. The contact systems can be divided into two subcategories: Schottky and Ohmic ones. The latter will be discussed, in detail.

When discussing Schottky-effect the work function of metals is first taken into consideration. The work function is the difference between vacuum level and Fermi level of energy. This energy (exit work) is necessary for an electron to exit the surface of a metal and leave to the free space. The I-V characteristics of a Schottky contact is asymmetric, the Ohmic contact has a linear I-V characteristics, thus the

latter is independent of voltage polarity. In practice, a contact is considered Ohmic, if the voltage drop of metal-semiconductor transition is less than that of the bulk semiconductor. The Ohmic contact can be replaced by  $R_c$  contact resistance.

$$R_c = \left( \frac{dJ}{dV} \right)^{-1} \Big|_{V=0} \quad (1)$$

where  $J$  is current density and  $V$  is the voltage drop. The value of contact resistance in case of medium doped n semiconductor-metal transition is largely determined by thermal emission, thus:

$$R_c = \frac{k_B}{q \cdot A \cdot T} * e^{\frac{q \cdot \Phi_{Bn}}{k_B \cdot T}} \quad (2)$$

Equation (2) demonstrates that if the goal was to attain a low resistance then the lowest potential barrier must be attained at the metal-semiconductor transition. If the Ohmic contact is strongly doped then field emission (tunnel effect) is the dominant component. In the latter case contact resistance can be expressed as

$$R_c \approx e^{\left( \frac{2 \cdot \Phi_{Bn}}{h} \right) * \left( \sqrt{\frac{\epsilon_0 \cdot \epsilon_s \cdot m_0}{N_D}} \right)} \quad (3)$$

Ohmic contact can be constructed several ways [12]. One possible solution is to choose a metal that has less work function than that of the n type semiconductor, thus the potential barrier between the metal and the compound semiconductor is thin enough that the electrons can tunnel through it in both directions. Another possible solution is to prepare a thin strongly doped layer of the same material as that of the substrate. This way a  $n^{++}/n$  or a  $p^{++}/p$  strongly doped weakly doped transition zone is prepared that decrease the thickness of metal/compound semiconductor potential barrier. Thus, the current flows thru the potential barrier via tunnel effect, because of the thin potential barrier and the low contact resistance. The third possible solution is to "simulate" gradual heterojunction with small band gap material. This means that  $n^{++}$ -InAs/n-GaAs or  $n^+$ Ge/n-GaAs heterojunctions are formed by MBE technology. The fourth possible solution is to apply a not alloyed superlattice with short lattice constant. This structure contains GaN and small band gap InN layers. The latter is inserted between GaN layers in a sandwich like structure with InN cover layer that forms Ohmic contact with the GaN. The fifth solution is to increase the number of recombination centers on the surface of semiconductors with surface roughening. This way the surface acts as an infinite drain of majority charge carriers of the contact.

In addition to the high energy radiation damage, the incorporation of chemical contaminants into the semiconductor these recomibnation centers may cause the Fermi-level pinning [13] [14] [15]. This phenomenon may occur in bulk material, in the interface layer and on the surface as well.

In bulk material the Fermi-level may move between the valence band and conductance band. Generally electrically active crystal defects influence the Fermi level as well. Crystal defects that act as donors prevent other defects from acting as

acceptors. These defects free electrons and push Fermi level upwards in the band gap, meanwhile other defects trap electrons and push Fermi level downwards.

Forming a clean surface causes discontinuity in the external potential that leads to occurrence of surface states. One must differentiate from mathematical point of view between the Shockley and Tamm states. The former stems from the pseudo free electron approximation, whence the latter stems from tight binding approximation. These states occur in high concentration that leads to Fermi-level pinning. The work function is almost independent of the location of bulk Fermi-level (doping level) which may be considered as pinned [16].

The study of Fermi level pinning near the interface is quite complicated, because of the multiple material on one hand and the several growing methods on the other hand. The barrier between the metal and semiconductor can be determined with the Schottky-Mott rule. This rule states that the thickness of the barrier is proportional with the difference of vacuum work function of the metal and the vacuum electron affinity of the semiconductor. This condition, called Schottky limit, is valid if there was no charge transfer between the metal and the semiconductor and there was no Fermi level pinning. Most of the materials do not show the phenomenon, because electric states are formed in the band gap of the semiconductor. These states contribute to charge transfer between the two materials and an electrostatic dipole is formed at the interface. The height of Schottky barrier is independent of work function and the Fermi level may be considered bended in this case. This condition is the Bardeen limit.

### 2.1.1 I-V Characteristics

The I-V characteristics of Schottky contacts can be measured in several ways. The possible methods are (1) measuring the photo reaction, (2) measuring I-V itself, and (3) and measuring C-V characteristics.

Similarly, the  $r_c$  specific contact resistance can be measured with multiple methods. Four ways of the possibilities [17] are (1) Cox-Strack method, (2) four point method, (3) Schottky extrapolation method, (4) transmission line method. In case of constant current density and homogenous surface of contact the  $R_c$  contact resistance may be obtained as:

$$R_c = \frac{r_c}{A} \quad (4)$$

The measured  $R$  resistance is approximately equal to  $R_c$  resistance in case of the most geometry of contact if  $r_c \geq 0.01 \Omega \cdot \text{cm}^2$ . For smaller values of  $r_c$  one must take into consideration the  $R_b$  spread resistance of the semiconductor and  $R_0$  resistance of contact wires and the bulk resistance of the substrate of the semiconductor. For this reason the measured  $R$  resistance is:

$$R = R_c + R_b + R_0 \quad (5)$$

where  $R_b$  and  $R_0$  depends on the geometry of metal/compound semiconductor.

It was supposed in the case of Cox-Strack method, that the contact is a circle with radius  $a$ , n-type film layer with specific resistance  $\rho$  and thickness of  $t$  [17] [18]. The surface resistance of the layer can be calculated as:

$$R_b = \frac{\rho}{a} * F \quad (6)$$

Where  $F$  is the function of  $a/t$  ratio. Experimentally, it was found that this function is approximately

$$F\left(\frac{a}{t}\right) = \frac{1}{\pi} * \arctan\left(\frac{2*t}{a}\right) \quad (7)$$

It may be necessary to determine  $F$  more exactly in several cases [19]. If this value is known then the specific contact resistance will be:

$$r_c = \pi * a^2 * \left(R - \frac{\rho}{a} * F\left(\frac{a}{t}\right) - R_0\right) \quad (8)$$

It is necessary to metallize only one side of the slice, when using the four point method for obtaining  $r_c$  [20]. The thickness of the layer is  $t$ . The layer can be epitaxial layer on semiconductor substrate or uniformly doped bulk material. The specific resistance in this case will be:

$$r_c = \pi * a^2 * \left(\frac{V_1}{l} - \frac{V_2}{l} - \frac{\rho}{a} * F\left(\frac{a}{t}\right)\right) \quad (9)$$

The potential distribution on the surface is rather logarithmic than exponential according to other authors [21]. The specific contact resistance will be in this case:

$$r_c = \pi * a^2 * \left(\frac{V_1}{l} - \frac{V_2}{l} * \frac{\ln\left(\frac{3*s}{2*a} \frac{1}{2}\right)}{2*\ln 2} - \frac{\rho}{a} * F\left(\frac{a}{t}\right)\right) \quad (10)$$

where  $v_1$  and  $v_2$  are the distance between the measurement point.

The crucial point of the Shokley method [22] [23], that  $V(x)$  voltage drop is measured along the surface of the semiconductor layer with coplanar ohmic contacts. The extrapolated  $V_0$  voltage is used through contacts and this way the  $r_c$  is found. Due to the  $R_s$  sheet resistance the contact resistance is not zero. The current is not distributed uniformly but concentrates under the contacts. The  $r_c$  contact resistance can be calculated by the extrapolation of linear voltage drop between two contacts, thus

$$r_c = R_b * L_T^2 \quad (11)$$

where  $L_T$  is the so called transferlength that in turn can be calculated with the following expression  $L_T = -x / \ln(V(x)/V_0)$ .

The planar contact is considered a resistive power line according to the power line method [24] [25] [26]. The resistance in this model is the can be calculated from a uniform  $R_s$  sheet resistance and specific  $r_c$  contact resistance. The  $R_e$  total resistance can be calculated as:

$$R_e = \frac{(r_c * R_s)^{\frac{1}{2}}}{W} * \coth \left( d * \left( \frac{R_s}{r_c} \right)^{\frac{1}{2}} \right) \quad (12)$$

where  $W$  is the width and is the  $d$  length of the power line. Since generally  $d * (R_s/R_c)^{\frac{1}{2}}$  the  $r_c$  contact resistance can be calculated as:

$$r_c = \frac{R_e^2 * W^2}{R_s} \quad (13)$$

The I-V characteristics can be visualized on the so-called Gummel plot as well (Fig. 3) [27]. The base and collector current are shown at the same time as a function of base-emitter voltage. The vertical scale (current scale) is logarithmic. A lot of diode parameters can be calculated using this chart, eg. the DC amplification [28] or the factor of ideality [29]. The value of the latter can imply the presence of recombination centers of volume or those of surface. The recombination centers can cause various problems (eg. Fermi-level pinning).

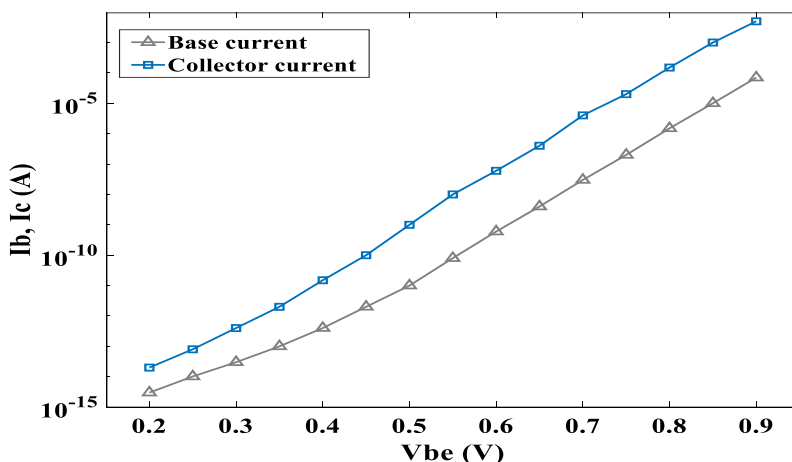


Figure 3

Gummel plot (source: [28])

Another possibility for examining the metal/compound semiconductor transition zone is the capacitance transient spectroscopy [30]. The crucial point of this method is the monitoring temporal change of charge density in the depleted zone of the diode. The thickness of this region is independent of the charge density. The thermal emission of the fixed position charge carriers causes capacitance change in the space-charge. This way information is received on trap states, and trap activation energy, the cross section of trap states and the concentration of traps. The capacitance of depleted layer changes due to thermal emission as follows:

$$C(t) = C_r * \left( 1 - \frac{n\tau_0}{2 * N_D} * e^{\left( -\frac{t}{\tau_e} \right)} \right) \quad (14)$$

where the  $n_{T0}$  is the density of filled traps at  $t = 0$  sec,  $C_r$  is the capacity of the diode if all the traps are empty at  $V_r$  voltage,  $\tau_e$  is the time constant of emission ( $\tau_e = 1 / e_n$ , where  $e_n$  is the emission ratio). One variety of the process is the SCTS method [31].

Deep-level transient spectroscopy, DLTS is a robust and widely used measurement method for determining the electrically active traps in the semiconductor [32] [33]. The DLTS is a correlation method where the transient of the capacity is multiplied with a correlation function (the signal of reference) and the product will be integrated.

Several parameters can be measure several parameters as the activation energy of defects, the trap cross sections and the density of traps.

There are no measurable surface and induced states and the metal/compound semiconductor transition zone is charge neutral in an ideal case [34]. Unfortunately this is not so in the case of eg. GaAs and several other semiconductor.

### 3 Technological Aspects of the Contacts

#### 3.1 Metallization

As it was mentioned in section 2.1. the contacts have important role regarding the connection of the device and its environment. This is essential at Ohmic contacts, because in the case of several devices and several circuit applications the examination of physical and electric properties of bulk material requires good quality Ohmic contacts [35].

The Ohmic contacts can be fabricated in two ways [36]: (1) any metals deposited onto semiconductor the contact will be Ohmic (in situ ohmic contacts), (2) if the deposited metal is annealed properly then it will be Ohmic. In the latter case it is crucial to take in consideration: (1) the decomposition the surface of GaAs with the possible vaporizing of As (2) the deviation in reactivity of GaAs that depends on the initial composition of the compound semiconductor (stoichiometric ratio, presence of remaining oxides, contaminations, passivating chemical elements).

The change of I—V characteristics of some Ohmic contacts grown on n-GaAs and p-GaAs will be examined as result of annealing process.

Firstly, contacts made of gold on the surface of GaAs was examined [37]. On such solution is the application of Au-Ge/In Ohmic contacts on n-GaAs substrate [36]. One system of this kind is shown in Fig. 4 before annealing (A) and after annealing at 495 °C for 5 minutes (B).



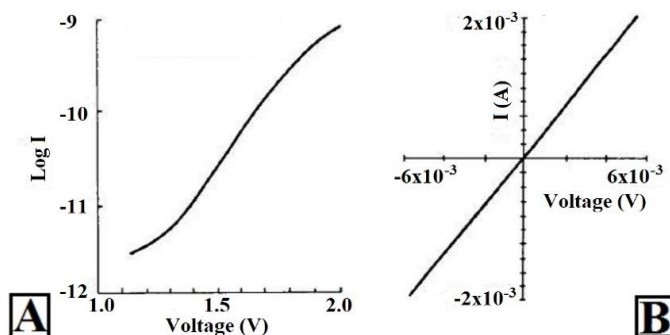


Figure 4

I-V characteristics of Au-Ge/In ohmic contact on n-GaAs substrate before annealing (A) and after annealing at 495 °C for 5 minutes (B)

A problem is that this metal reacts with GaAs at a relatively low temperature (above 350 °C). Further problems are the occurrence of all the three, the parasitic substrate currents and the deep and shallow trap states [38]. For this reason several other solutions were found to substitute Au metallization.

Cu was used instead of Au in one experiment [39]. A Pd/Ge/Cu metallization was applied to n-type GaAs and Pt/Ti/Pt/Cu metallization was applied to p-type GaAs. A comparison of Au and Cu based metallization on n-GaAs (Fig. 5/A) and on p-GaAs (Fig. 5/B) substrate.

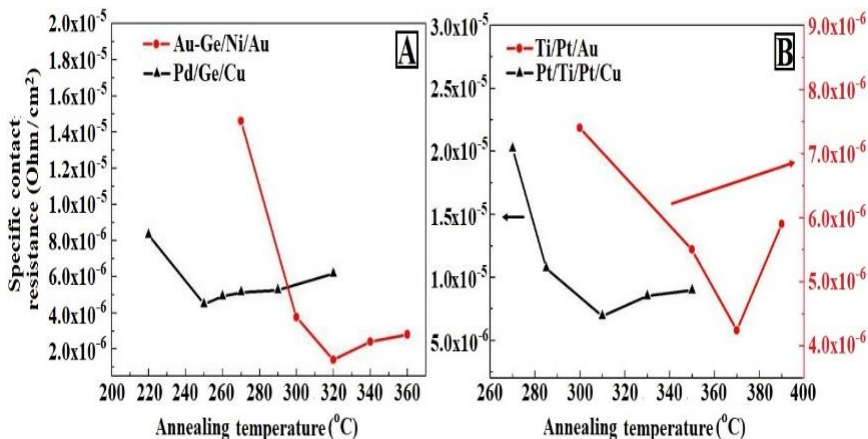


Figure 5

Comparison of Au and Cu metallization on n-GaAs (A) and on p-GaAs (B) substrate (source: [40])

The other possible solution also with Cu is Pd/Ge/Cu metallization on n-GaAs substrate [40]. This paper describes an experiment annealing in N gas environment for 20 minutes between 150 °C and 400 °C. The authors examined the resistance of the contact as a function of annealing temperature with different Pd (Fig. 6/A) and different Ge layer thicknesses (Fig. 6/B).

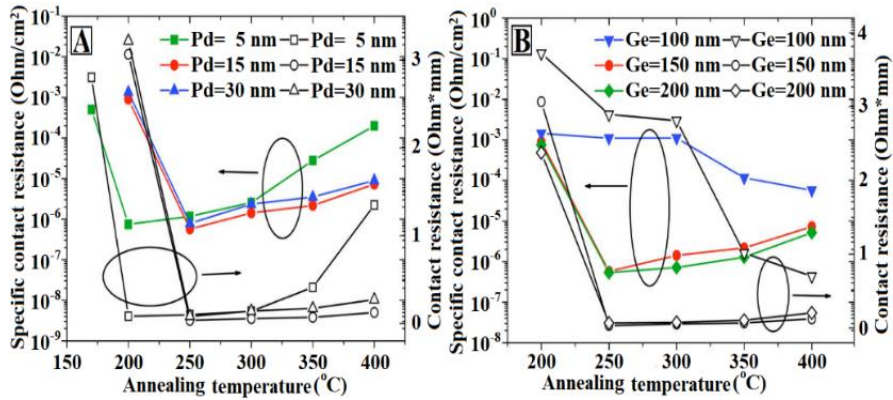


Figure 6

Comparison of Cu based metallizations as a function of thickness of Pd layer (A) and thickness of the Ge layer (B) (source: [41])

A third possible solution, a non-copper based one, is the NiGe metallization on n-GaAs [41]. The authors of this paper examined several samples with different metal layer thickness. Sample 3 shown in Fig. 7 the Ni layer is 75 nm and the Ge layer is 90 nm thick after 5 minutes annealing. The sample shown on Fig. 8 the authors applied 400 °C isotherm annealing and the specific resistance was measured at identical time intervals. Sample 3 had a Ni layer thickness of 75 nm and that of Ge 90 nm, whence sample 5 had 15 nm thick first Ni layer and 72 nm Ge layer and the second Ni layer was 75 nm.

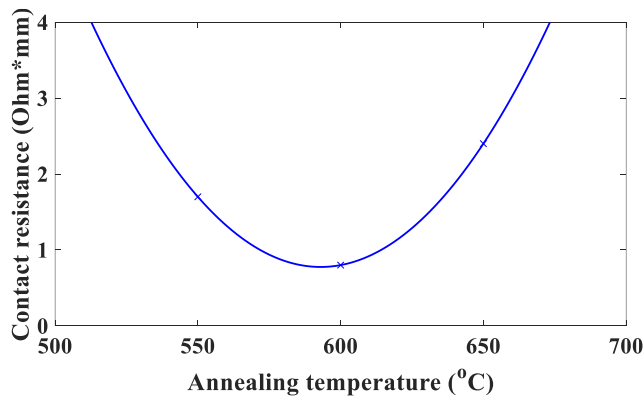


Figure 7

The Ni layer is 75 nm thick and the Ge layer 90 nm thick, after 5 minutes annealing between 550 °C and 650 °C (source: [42])

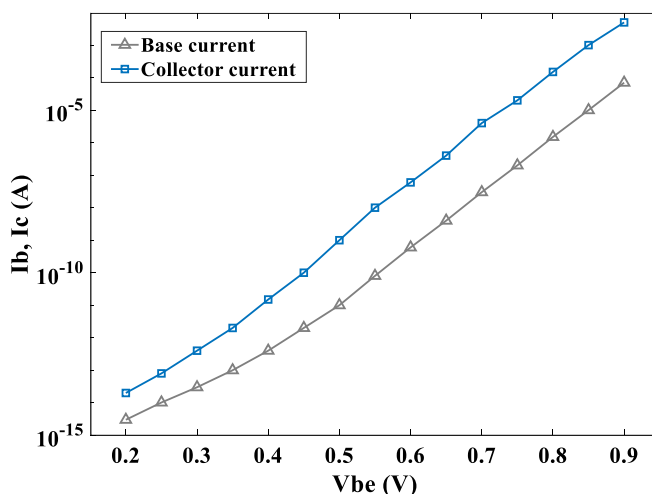


Figure 8

The contact resistance as a function of annealing time period (NiGe metallization), in case of sample 3 and sample 5, in 400 °C isotherm annealing (source: [42])

The fourth possible solution is application of NiSiW metallization [42]. The first Ni layer is 30 nm thick, the Si layer is 40 nm thick, the second Ni layer is 15 nm thick, thus the W layer is 40 nm in sample shown in Fig. 9. The specific contact resistance is shown as a function of temperature of annealing (Fig. 9/A) and as a function of time interval of annealing (Fig. 9/B).

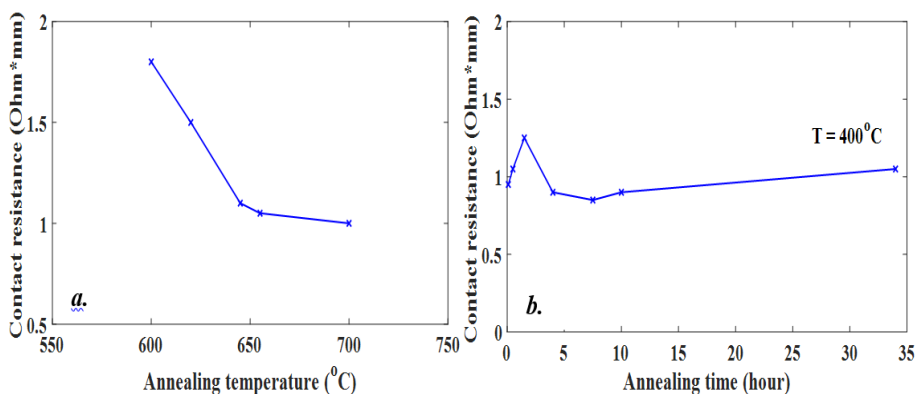


Figure 9

Values of contact resistance as a function of annealing time (NiSiW metallization), 400 °C isotherm annealing. The contact resistance is shown as a function of annealing temperature (A) and as a function of annealing time (B). (source: [42])

The fifth possible solution is application of Pd/Sn metallization on n-GaAs substrate [43]. The authors of the above mentioned paper applied a 32.4 nm thick Pd layer

and a 150 nm thick SN layer as metallization and the time interval of annealing was 30 minutes. The contact resistance- annealing temperature diagram can be seen in Fig. 10.

The sixth possible solution is to apply Pd/Ge metallization on n-GaAs substrate [44]. The sample was annealed for 30 minutes in N gas environment between 200 °C and 250 °C as mentioned in this paper. The contact showed increasingly ohmic characteristics with increasing annealing temperature as shown in Fig. 11/A. The contact resistance- annealing temperature diagram of the same material system is shown in Fig. 11/B.

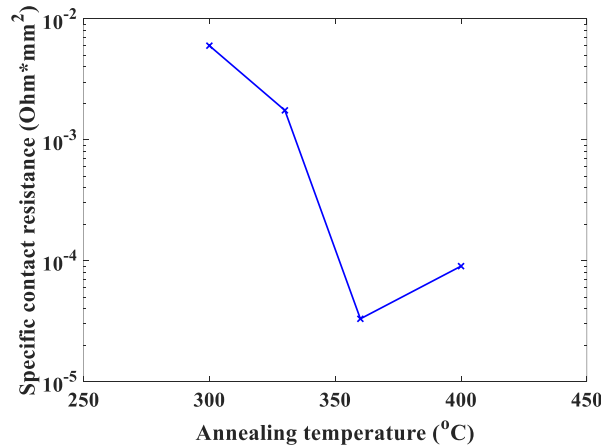


Figure 10

Contact resistance – annealing temperature diagram of Pd/Sn metallization (source: [43])

The selection of the contact material for compound semiconductors and the determining the appropriate thermal profile for different contact metallizations is a problematic area, and several researches are in progress. The main problem is that when a simple metal is used for GaAs metallization the system is instable in terms chemistry and thermal phenomena [45].

During the formation process of contact the extent to which the metal wets the surface under consideration has an important role. The wetting is the attachment ability of liquid phase material to a solid surface. This attachment ability is the macroscopic approach of intermolecular effects [46] [47] [48]. The degree of wetting depends on the balance of adhesive and cohesive forces. Wetting is related to solid, liquid and gaseous phases as well. Wetting has an important role when the binding of two different materials is studied. Wetting has two types, reactive and non-reactive [49].

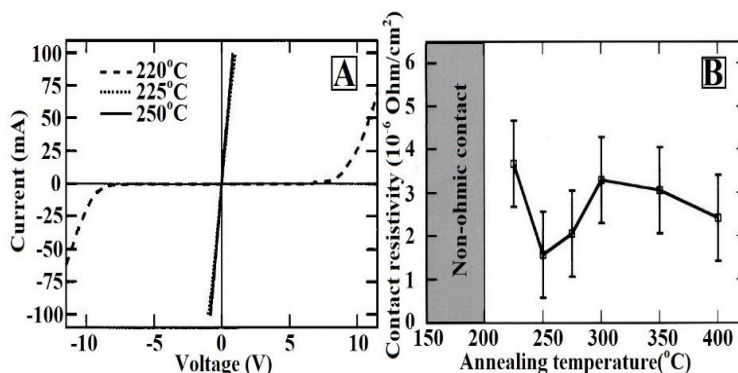


Figure 11

I-V diagram of Pd/Ge metallization with annealing temperature as parameter (A) and the contact resistance as a function of annealing temperature of the material system (B) (source: [44])

The properties of Ohmic contacts depend on the applied material system and the temperature of the applied annealing [50]. For this reason it is necessary to take into consideration two factors when examining the metal/compound semiconductor system during the annealing process [51] [35]. The first factor is the surface decomposition at relatively low temperature. It is the vaporization of volatile component. In case of GaAs the As is the volatile component [52] [53] [54]. The second factor is the varying reactivity of GaAs surface that depends on the initial structure of the substrate (stoichiometry, contaminants, residual oxides and presence of passivating materials). This temperature dependence was examined for material systems of Au/Pd [55], Pd [54], Au/Ge [56] [57] and Au/Ge/Ni [57] [58] [59] [60]. During the annealing process the volatile component evaporates. The volatile component is As in case of GaAs, and P in case of InP [55]. The result of thermal mutual effect in case of a thin layer system and compound semiconductor (eg. InP) was observed by scanning electron microscope [54] [61] [62] [63] [64] [65] [66]. The samples were examined in heated sample holder. Different surface features were produced by different material science processes (eg. Surface migration). The goal of the researchers was to determine the connection between the conditions of interaction, the materials involved and the attributes of the substrate. The temperature dependence of vaporized volatile component was examined in the given experimental arrangement. The amount of the vaporized component was measured by a quadrupole mass spectrometer (EGA – evolved gas analysis). The electrical parameters of the fabricated contact were deduced then.

### 3.2 Geometrical Investigation

The metallization patterns that formed on the surface of GaAs contact can be described by multiple models. These models can be divided into two groups, the continuum and atomic ones. Such a nonlinear continuum model is the Kardar-Parisi-Zhang equation [67] [68] [69]:

$$\frac{\partial h(x,t)}{\partial t} = \nu * \Delta h(x,t) + \frac{\lambda}{2} * (\nabla h(x,t))^2 + F + \eta(x,t) \quad (15)$$

where  $\nu$  is the surface tension,  $t$  is the time,  $h(x,t)$  is the height of interface at point  $x$ ,  $\lambda$  is the wavelength,  $F$  is the incoming atomic flux, the  $\eta(x,t)$  is the noise component (flux of the random inbound atoms. Atomic model eg. the so-called Kinetic Monte-Carlo algorithm [70] [71] [72], or the kinetic mean field model [73].

The surface can be characterized, in addition to surface roughness, in other ways, eg. examining the surface patterns. Many surface pattern investigations are in the literature in case of GaAs substrate [54] [55] [57] and in case of InP substrate [74] [58] [61] as well. The biggest obstacle of the examination is the segmentation of clusters a difficult task to do. The contrast may be weak thus it is hard to separate the cluster from the background according to tone thresholds. This problem can be solved in multiple ways, eg. by the GOFM (grade of membership method) [75] [76], or by fractal mathematical methods [77] [78] [79], or by structural entropy [80] [81].

The crucial step of grade of membership method (GOFM) is to separate the surface and the structure with the subsequent function when examining the given surface pattern:

$$G(x) = \frac{1}{\sum_{j=1}^n \left( \frac{(x-v_j)^2}{(x-v_j)^2} \right)^{\frac{1}{m-1}}} \quad (16)$$

where  $x$  is the brightness of the pixel,  $v_j$  is the brightness of the pixel in the center of  $j^{\text{th}}$  cluster,  $n$  is the number of the clusters,  $m$  is the membership weight.

The surface patterns can be analysed by fractal theory as well. The fractals are infinitely complex, in terms of statistics „self similar”, mathematical objects. In the countless different formation of fractals, there is at least one repetition that can be described by mathematical toolset [77] [78] [79].

The analyses utilizing the fractal theory can be found in [62] [74]. These analyses are based on in situ SEM images of the surface of contacts during the annealing process. These pictures were taken by L. Dobos *et al.*, in a converted SEM. They provided the technical possibility of fast annealing processes at maximum of 700 °C. Bitmap (BMP) files were obtained by digitalizing SEM images. Further, the BMP images were processed by software [63].

The surface of a given, non-continuous thin layer is considered to be of fractal pattern if the black and white image of the surface has dimension between 1 and 2. The more regular and the more complete the coverage of the plane, the closer the dimension gets to 2.

The most widespread method of measurement of fractal dimensions of fractals in terms of mathematics (eg. bicolor images) is the so-called box-counting methodology elaborated by B. Mandelbrot [82] and Hausdorff [83].

In the course of our research Au, Pd and Au/Pd thin layers were deposited onto InP surface [74]. The data of the material system can be found in Table 1.

Table 1  
The data of the examined material system

Orientation of substrate	Au/InP(111)	Pd/InP(100)	Au/Pd InP(100)
Layer thickness [nm]	60	50	85/50

Our goal was to thoroughly examine the surface morphology of Au, Pd and Au/Pd layers in terms of fractal patterns.

During the research the original records were cut. During the next step the records were converted to binary format according to Hausdorff measure. The boxes of diameter  $n$  necessary to cover the white pixels, were counted. This step was repeated with boxes of diameters of  $n/2$ , and so on until boxes of one pixel were reached.

If the logarithm of box count is plotted on a diagram as a function of number of the steps and a line is matched onto these points, then the fractal dimension is obtained.

In addition to fractal geometry, the same surfaces were examined by both filling factor and structural entropy methods. The structural entropy [80] [81] [84] [85] determines the localization type of probability distribution defined on lattices. In other words, this method defines the function according which the agglomerations of the probability distribution fade.

Let us have  $n$  lattice points of which only  $m$  points are filled. The filling factors are identical  $p_i = 1/m$  and these values are  $p_i = 0$  for the rest of lattice points. The structural entropy is that part of the entropy of the system which tells us accordingly, which functions, in the filled lattice, points decay. The shape of the fading is characterized by structural entropy which has the algebraic expression:

$$S_{str} = s - \ln d = \sum_{i=1}^n p_i * \ln p_i - \ln \frac{1}{\sum_{i=1}^n p_i^2} \quad (17)$$

In case of two valued step like distribution the value will be zero because the Shannon entropy will be exactly  $\ln d$ . For this reason, these calculations were carried out on grayscale images.

A variable that indicates the mean filling of a lattice point was introduced:

$$q = \frac{d}{n} = \frac{1}{n \sum_{i=1}^n p_i^2} \quad (18)$$

This variable is the filling ratio. If structural entropy was plotted as a function of filling ratio then it is observed that the graph of each fading functions (eg. the Gaussian function, the power functions etc.) is a well-defined curve on the  $Q - S_{str}$  plane. If it was examined that which function fits the point of the distribution, then the type of fading can be determined [80] [86]. The underlying theory is detailed in [81]. The shaded area can be characterized by inequalities  $0 < q < 1$  and  $0 < S_{str} <$

$-\log q$  (Fig. 12). The structural entropy and localization factor can be used for analysis of AFM and in addition to, SEM records [87] [90].

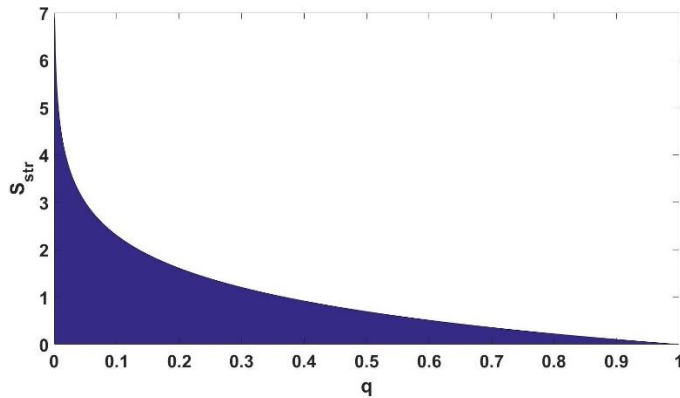


Figure 12

Allowed region of structural entropy plot

In the Fig. 13 the surface of the Au (60 nm) layer on GaAs (100) substrate (Fig. 13/a) at 400 °C temperature, (Fig. 13/b) at 500 °C temperature (Fig. 13/c) at 630 °C temperature (magnitude is 500x).

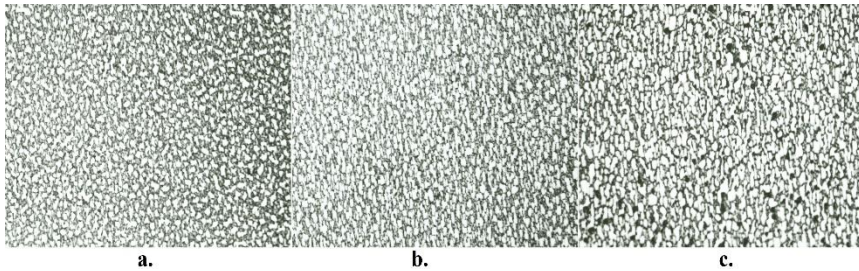


Figure 13

The surface of the Au (60 nm) layer on GaAs (100) substrate (a) at 400 °C temperature, (b) at 500 °C temperature, (c) at 630 °C temperature (magnitude: 500x)

In the next two subchapters the Au/GaAs and Au/TiN/GaAs material systems are characterized by fractal dimension and by structural entropy as well.

### 3.2.1 Au/GaAs Material System

In the Au/GaAs system, the change of the fractal dimensions is shown in the Fig. 14, between 440 °C and 600 °C. In case of Fig. 14/b, the width of the Au layer is 40 nm and the fractal dimension decreases significantly in the function of the temperature. In case of Fig. 14/b the width of the Au layer is 60 nm and the fractal dimension is nearly constant. Probably the reason of this phenomena is the decreasing of the fractal dimension, which is caused by the evaporation of the illicit



component of the substrate (this is the As component, in case of GaAs). As it is shown in the Fig. 14, in case of the 40 nm Au layer thickness (Fig. 14/a), the evaporation of the illicit component is larger than in the case of the 60 nm Au layer (Fig. 14/b). According to this result, this phenomenon depends on the thickness of the Au layer.

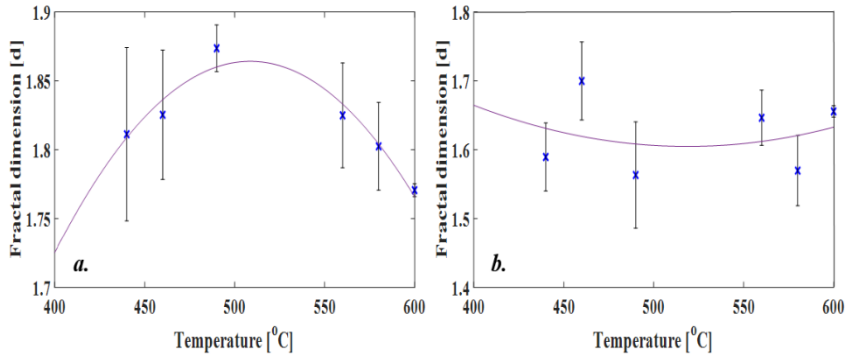


Figure 14

The change of the fractal dimension between 440 °C and 600 °C.  
The width of the Au layer is (a) 40 nm and (b) 60 nm.

In Fig. 15, the structural entropy is shown, in case of 40 nm (Fig. 15/a) and in case of 60 nm (Fig. 15/b) Au layer width. The investigated temperature is 500 °C. Based on Fig. 15, it is apparent, that the decay of the structural entropy is slower than the Gaussian function.

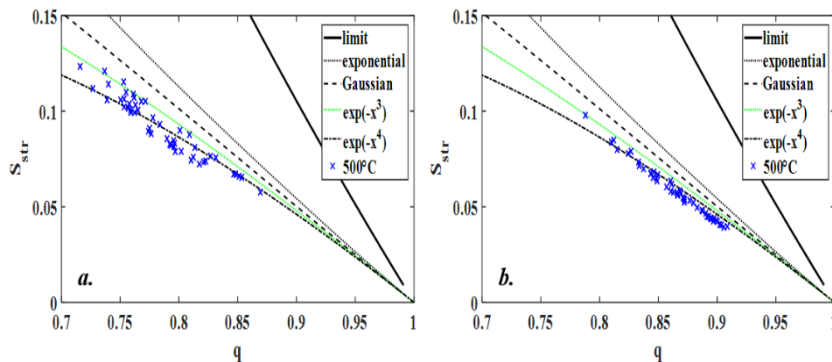


Figure 15

The structural entropy of the Au/GaAs system in 500 °C temperature.  
The width of the Au layer is (a) 40 nm and (b) 60 nm.

As it is visible in the Fig. 16, the localization factor between 440 °C and 600 °C also depends on the width of the Au layer. In case of the Fig. 16/b (60 nm Au layer width) the steepness is twice larger as the Fig. 16/a (40 nm Au layer width), between 440 °C and 472 °C, 472 °C and 504 °C, 504 °C and 536 °C.

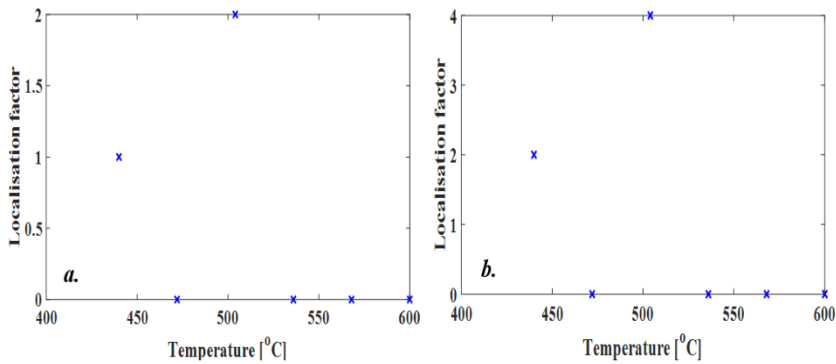


Figure 16

The change of the localization factor between 440 °C and 600 °C.

The width of the Au layer is (a) 40 nm and (b) 60 nm.

### 3.2.2 The Au-TiN/GaAs Material System

As it is shown in the Fig. 17/a, the fractal dimension in the 15 nm thick Au-TiN/GaAs layer is increasing in the function of the temperature. Unfortunately, the reason of this phenomenon is not known. In the Fig. 17/b, the fractal dimension decreases in the function of the temperature. The width of the Au-TiN layer is 25 nm, unfortunately more samples were not available.

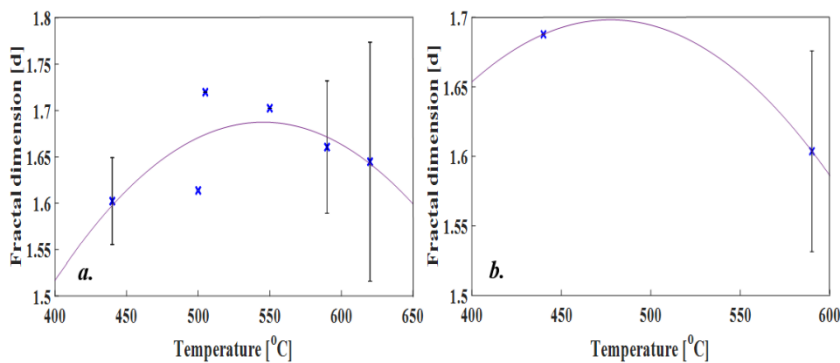


Figure 17

The change of the fractal dimension between 440 °C and 600 °C.

The width of the Au-TiN layer is (a) 15 nm and (b) 25 nm.

Similar to the previous material system, in the Fig. 18 it is also visible, that the structural entropy depends on the width of the TiN layer. The investigated temperature is 500 °C. It is apparent, that the decay of the exponential curves structural entropy decays as a Gaussian (Fig. 18/b) or third-order exponential function (Fig. 18/a).

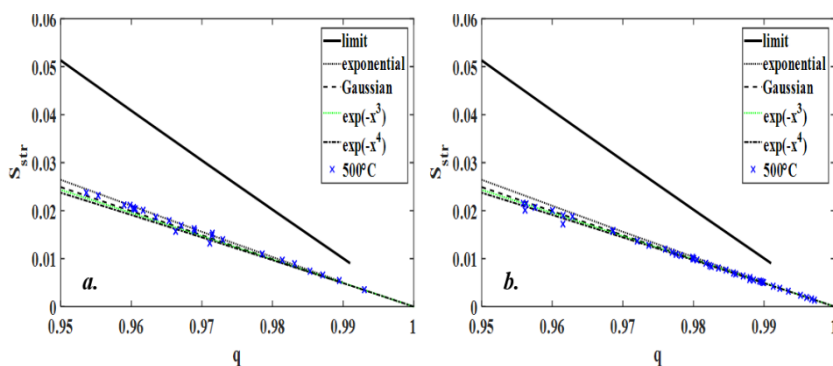


Figure 18

The structural entropy of the Au-TiN/GaAs in 500 °C.  
The width of the Au-TiN layer is (a) 15 nm and (b) 25 nm.

As it is visible in the Fig. 19, the localization factor of the 15 nm thick Au-TiN/GaAs material system is third-order (Fig. 19/a). The localization factor of the 25 nm thick Au-TiN/GaAs material system is Gaussian (Fig. 19/b). The values of the localization factors are constant, so – in the investigated temperature range – of the localization factors are independent from the temperature.

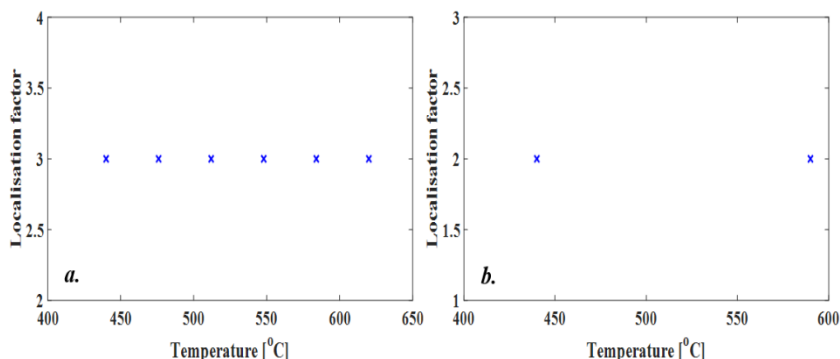


Figure 19

The change of the localization factor between 440 °C and 600 °C.  
The width of the Au-TiN layer is (A) 15 nm and (B) 25 nm.

## Conclusion

This paper focused on the electric and morphologic attributes of metal/compound semiconductor contacts. Detailed results were presented on electric qualities of Ohmic and Schottky contacts, on measurement technology and on different types of metallization, after the introduction. An examination of patterns on the surface of metallization was also explored. With the fabrication of solar cells in mind, the crucial point is the formation of internally homogeneous Ohmic contacts. The electric features and factors of lateral inhomogeneity were summarized and the

obtained morphologies were examined. The next phase of our work will be the relationships of different morphologies and their electric qualities.

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