

# Switching dynamics in Al/InAs nanowire-based gate-controlled superconducting switch

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The observation of the gate-controlled supercurrent (GCS) effect in superconducting nanostructures increased the hopes for realizing a superconducting equivalent of semiconductor field-effect transistors. However, recent works attribute this effect to various leakage-based scenarios, giving rise to a debate on its origin. A proper understanding of the microscopic process underlying the GCS effect and the relevant time scales would be beneficial to evaluate the possible applications. In this work, we observed gate-induced two-level fluctuations between the superconducting state and normal state in Al/InAs nanowires (NWs). Noise correlation measurements show a strong correlation with leakage current fluctuations. The time-domain measurements show that these fluctuations have Poissonian statistics. Our detailed analysis of the leakage current measurements reveals that it is consistent with the stress-induced leakage current (SILC), in which inelastic tunneling with phonon generation is the predominant transport mechanism. Our findings shed light on the microscopic origin of the GCS effect and give deeper insight into the switching dynamics of the superconducting NW under the influence of the strong gate voltage.

In 2018, De Simoni et al.<sup>1</sup> observed a monotonic suppression of the supercurrent in titanium (Ti) NWs by increasing the voltage beyond a certain threshold at a nearby gate (side or back) electrode. With further increases in the gate voltage, the supercurrent is fully suppressed, and the device is switched to the normal state, providing a superconducting equivalent of semiconductor CMOS transistors with an expected high switching speed and low power consumption. Moreover, the structure of gate-controlled superconducting nanodevices

can be readily scaled up with greater compatibility for interfacing with CMOS transistors in comparison to alternative superconducting devices<sup>2–5</sup>. The earlier experimental observations of the GCS were associated with various unique fingerprints, which were attributed to the influence of the external  $E$ -field<sup>1,6–17</sup>. Later on, most of these fingerprints were observed in other works suggesting leakage current-based scenarios<sup>18–24</sup>. Furthermore, the different experimental conditions, e.g., superconducting material, substrate, and device

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configuration, make it hard to compare different works<sup>25,26</sup>. As a result, the microscopic origin of the GCS remains controversial. In particular, the role of the leakage current is the key point in the ongoing debate between different studies. Therefore, it will be necessary to understand the microscopic origin behind the GCS effect to assess the reliability of the GCS-based devices to compete with semiconductor technology in various applications.

The low-frequency  $1/f^\alpha$  noise is widely observed in various nanoelectronic devices<sup>27–30</sup>. Investigation of  $1/f^\alpha$  noise can provide valuable information and a deeper understanding of the transport mechanisms and the dominant sources of fluctuations in different nanodevices<sup>27–30</sup>. In addition, noise correlation measurements are very powerful techniques that can be used for probing the cross-correlation between different fluctuating quantities in such systems, which has proven to be successful, for example in the investigation of the bosonic or fermionic, or even the anyonic nature of charge carriers in two-dimensional electron gas<sup>31–34</sup>. In this work, we address the GCS effect in Al/InAs NWs with  $1/f^\alpha$  noise measurements for the first time. We chose Al/InAs NWs as they demonstrated a reliable GCS with fingerprints resembling those observed by metallic devices<sup>21</sup>. By carrying out cross-correlation measurements, we show that gate-induced fluctuations in the superconducting NW are directly related to time-dependent leakage current. Furthermore, we performed time-domain measurements to explore the statistics of these fluctuations and the relevant time scales. Finally, based on the detailed analysis of our results, we give a plausible explanation for the microscopic process behind the GCS in the Al/InAs gate-controlled superconducting switches.

## Results

### Device outline and gate influence

We have investigated the GCS in Al/InAs NW-based devices with the device configuration shown in the false-colored SEM image in Fig. 1a (see Methods for the fabrication details). Four Ti/Al contacts (blue) were deposited on top of Al/InAs NW (green) for quasi-four probe measurements. Two Ti/Au side gates (yellow) are placed on opposite sides of the NW and used for tuning the supercurrent in the NW. We first investigated the GCS effect by measuring the  $V-I$  characteristics of the device as a function of  $V_{\text{sg}}$  in both positive and negative gate polarities, as shown in Fig. 1b, which is similar to earlier observations<sup>21,23</sup>. As the bias current is swept from negative to positive polarity, there are two borderlines separating the superconducting state (white region) from the normal state regions (blue and red regions). These lower and upper borderlines represent the gate dependence of the retrapping current  $I_r$  and the switching current  $I_{\text{SW}}$ , respectively. At  $V_{\text{sg}} = 0$  V, the device switches to the normal state at  $I_{\text{SW}} \approx 6 \mu\text{A}$ , while it switches from the normal state to the superconducting state at  $I_r \approx 4.3 \mu\text{A}$ . As the device switches to the normal state, it shows a finite resistance  $R_n = 56 \Omega$ . This resistance can be attributed purely to switching of the Al shell to the normal state, as the  $I-V$  curve at  $V_{\text{sg}} = 0$  V (blue curve at Fig. 1d) of the device shows a single transition to the normal state in the entire bias current range in contrast with our previous work<sup>21</sup>. As  $V_{\text{sg}}$  increases in either positive or negative gate polarity,  $I_{\text{SW}}$  is suppressed from a certain threshold gate voltage  $V_{\text{sg,onset}} = 3.5$  V until it is fully quenched at the critical gate voltage,  $V_{\text{sg,offset}} \approx 6$  V. Since the thickness of the Al shell is 20 nm, which is an order of magnitude larger than the Thomas-Fermi length in Al, the electric field is fully screened by the superconducting shell, and it does not influence the InAs core. Consequently, the gate dependence of the supercurrent reflects the influence of the gating of the Al shell, with a negligible contribution from the proximitized InAs core. At the gate voltages, where  $I_{\text{SW}}$  is suppressed, a corresponding enhancement in the leakage current,  $I_{\text{leak}}$  is observed (see Fig. 1c), similar to what was reported in refs. 19,21–24. Figure 1d shows selected  $V-I$  curves at different gate voltages for the positive polarity of the

bias current and gate voltage and separated vertically for clarity. The  $V-I$  curve at  $V_{\text{sg}} = 0$  V (blue curve) shows a well-developed zero resistance below  $I_{\text{SW}}$ , while at higher gate voltages, e.g., at  $V_{\text{sg}} = 5$  V (green curve), finite voltage fluctuations across the NW are observed slightly below  $I_{\text{SW}}$  at the bias current values in the interval of [2,4]  $\mu\text{A}$ .

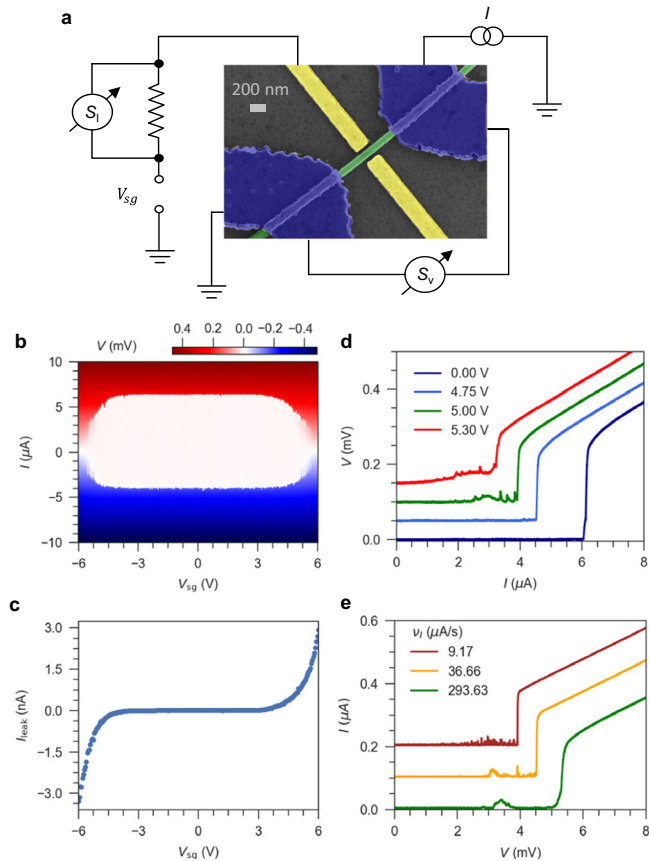
Figure 1e shows the  $V-I$  curve measured at  $V_{\text{sg}} = 5$  V with different current ramp speeds,  $v_i$ . At  $v_i = 9.17 \mu\text{A/s}$ , the  $V-I$  curve exhibits noisy region below  $I_{\text{SW}} \approx 6 \mu\text{A}$ . As  $v_i$  is increased up to 293.63  $\mu\text{A/s}$ , the NW device becomes less sensitive to these fluctuations, suggesting that the time scale of the fluctuations is the same order of magnitude as the time scale corresponding to the current ramping rate. It also implies that increasing gate voltage does not only suppresses  $I_{\text{SW}}$ , but also induces a dissipative region in which the voltage across the superconducting NW has dynamical fluctuations.

### Noise correlation measurements

Considering the ongoing debate regarding the origin of the GCS effect, it is valuable to investigate the correlation between gate-induced voltage fluctuations in the superconducting NW and the leakage current, both of which are simultaneously monitored in our experimental setup (see schematic of the measurement setup in Fig. 1a and details in Methods). To investigate this, we first studied the low-frequency fluctuations in the leakage current by measuring the power spectral density of the current noise  $S_I$  on the resistor  $R_G$  as a function of the applied gate voltage  $V_{\text{sg}}$  (see the Supporting Information).

To investigate the gate-induced voltage fluctuations in the NW device, we fixed  $V_{\text{sg}}$  at 5 V and measured simultaneously the spectral density of the leakage current noise  $S_I$  and the induced voltage noise  $S_V$  across the NW device as a function of the bias current (see the Supporting Information for complete measurements). Figure 2a shows the  $V-I$  curve of the NW device measured in parallel with the noise measurements. The colored arrows point to working points along the  $V-I$  curve where the behavior of the measured noise spectra of the NW device will be studied. These points are representative samples from the three characteristic regimes in which the  $V-I$  curve exhibits a pure superconducting state (dark and light blue arrows), voltage fluctuations below  $I_{\text{SW}}$  (light and dark green, red, and yellow arrows), and a pure normal state (brown arrow) with corresponding noise spectra of  $S_V$  shown in Fig. 2b. The noise spectra measured in the pure superconducting (dark and light blue curves) have the same amplitude as the background noise originating from the setup (black curve) measured at  $I = 0 \mu\text{A}$  and  $V_{\text{sg}} = 0$  V. Similarly, the noise spectrum measured in the normal state (brown curve) also has the same noise level within our experimental resolution. On the other hand, the noise spectra measured in the voltage fluctuation region are more than an order of magnitude larger. Interestingly, the noise spectrum  $S_V$  measured at  $I = 3.2 \mu\text{A}$  (dark green curve) has  $1/f$  dependence ( $\alpha = 1$ ), while the spectra at higher bias current values (light green, red, and yellow curves) have a steeper slope at higher frequencies ( $\alpha = 2$ ) resembling a Lorentzian spectrum (see the Supporting Information).

The cross-correlation between the leakage current noise and the induced noise in the NW was investigated in terms of the coherence  $C_{IV}$  (see Methods). If two signals are fully correlated, coherence has a value of 1, while for uncorrelated signals, it is 0. Figure 2c shows the coherence (averaged per frequency octave) between the two noise signals at different bias current values. The coherence measurements show that it has values of 0.3–0.8 for the light and dark green, yellow, and red curves, corresponding to the entire current region where the voltage fluctuation is observed, while it is  $C_{IV} < 0.2$  for the curves measured at the superconducting and normal states (see the complete measurements in the Supporting Information). This indicates that the voltage fluctuations observed in the superconducting wire are not independent, but they are strongly correlated with the current fluctuation of the leakage between the gate and the superconducting NW. This strong correlation was also confirmed by the time-domain



**Fig. 1 | Device outline and influence of the gate.** **a** A false-colored SEM image and schematic of the external measurement setup. Four Ti/Al contacts (blue) were deposited on top of Al/InAs NW (green) to perform quasi-four probe measurements. Two opposite side gates (yellow) made of Ti/Au were fabricated to investigate the GCS effect in the device. The leakage current is probed by measuring the voltage across the resistor  $R_G = 1\text{ M}\Omega$  connected in series with the gate. **b**  $V-I$  characteristics of the NW device as a function of  $V_{sg}$  in which the bias current  $I$  is swept from  $-10$  to  $10\ \mu\text{A}$ . The red and blue regions represent the normal state, while the white region corresponds to the superconducting state. **c** The corresponding  $I_{leak}$  as a function of  $V_{sg}$ . **d** Selected  $V-I$  curves extracted from **a** at different gate voltages in the positive polarity of the bias current and gate voltage. The curves are measured at  $v_l = 293.63\ \mu\text{A/s}$  (**e**)  $V-I$  curves measured at different current ramp speeds  $v_l$  at  $V_{sg} = 5\text{ V}$ . The curves are shifted vertically for clarity. The scattering in the switching current values for the green curves in panels **d** and **e** measured at the same current ramp speed can be attributed to the broad nonthermal switching current distribution induced by the applied gate voltage<sup>9,22–24</sup>.

measurements. Figure 2d shows the time-domain measurements for the fluctuations on the top of the average leakage current  $\Delta I_{leak}$  (gray curve) and the induced voltage fluctuations in the NW (red curve) at  $V_{sg} = 5\text{ V}$  and at  $I = 5.3\ \mu\text{A}$ . The time traces show that the leakage current fluctuates from a low to a high current state, whereas the voltage across the device changes from a zero-voltage state to a finite-voltage state. This strong correlation is a very robust effect as we have observed a high coherence between the leakage current noise and the induced voltage noise across the superconducting NW in three other devices (see the Supporting Information), which confirms the reproducibility of our results.

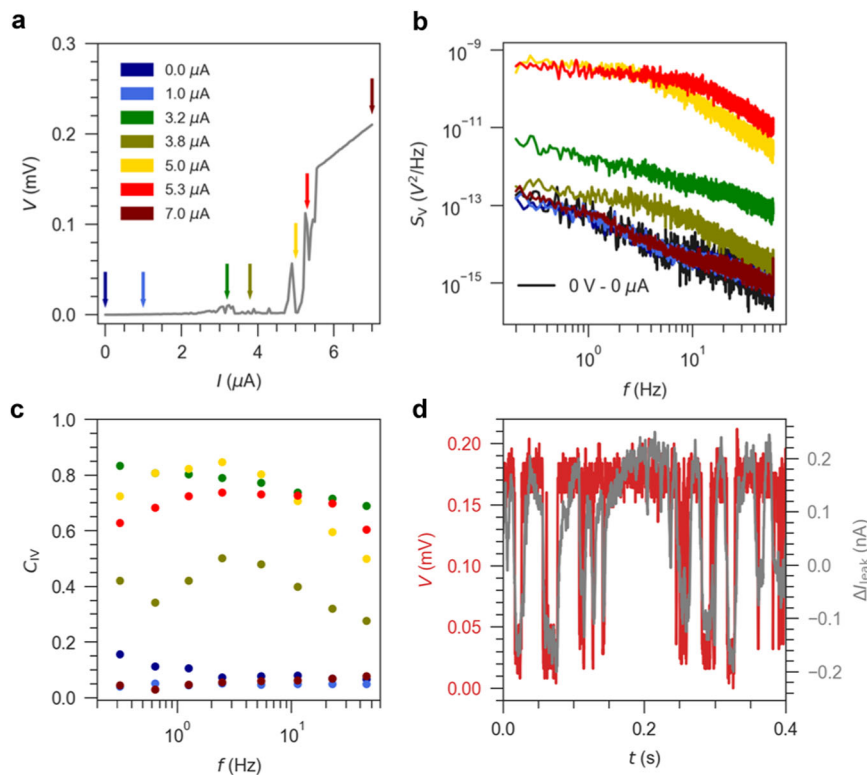
### Time-domain measurements

To understand the nature of the induced voltage fluctuations in the NW, we measured the voltage across the superconducting NW  $V$  as a function of time at a finite gate voltage and different bias current values. Figure 3a shows the time average  $V-I$  curve measured at  $V_{sg} = 5\text{ V}$ . The  $V-I$  curve is obtained by averaging a 119 s-long time trace for

each bias current value. The time traces were measured by an ultra-high frequency lock-in amplifier (See Methods) with a sampling rate of 27.5 kS/s. Figure 3b shows typical time traces of  $V$  at different bias current values in which the device exhibits a pure superconducting state (blue trace measured at  $0.48\ \mu\text{A}$ ), a pure normal state (red trace measured at  $5\ \mu\text{A}$ ), and the regime below  $I_{SW}$  (orange trace measured at  $4.2\ \mu\text{A}$ ), where the large voltage fluctuations have been observed. As expected, the time traces measured in the superconducting and normal states show a constant zero-voltage and finite-voltage across the device with time, respectively. On the other hand, the time trace measured in the voltage fluctuation regime shows that the device has voltage fluctuations between two well-defined values, as already seen in Fig. 2d. Figure 3c presents the distribution of the measured voltages constructed from the time traces and normalized by the maximum bin counts at  $I = 4.2\ \mu\text{A}$ . It shows a histogram with two peaks, one with a high probability at  $0\text{ V}$ , which we identify as the superconducting state. To understand the nature of the high voltage state, we set a threshold at  $V = 0.1\text{ mV}$ , as indicated by the gray dashed line between the two voltage states (see Fig. 2b, c). The voltage above the threshold was averaged for the whole period, denoted by  $\langle V_n \rangle$ . This average voltage was extracted for different bias currents in the region marked by the red dashed lines in Fig. 3a and plotted as a function of the corresponding bias current (see inset of Fig. 3a). The average voltage increases linearly with the bias current with a corresponding resistance of  $R \approx 80\ \Omega$  which is in the same order of magnitude as the normal state resistance measured at  $I > 4.5\ \mu\text{A}$  ( $R_n = 56\ \Omega$ ). This indicates that the high voltage state is the dissipative normal state, and the NW in the voltage fluctuation region oscillates between the superconducting and normal states. This is possible since, at  $V_{sg} = 5\text{ V}$ , the voltage fluctuations appear slightly below  $I_t$  (see the Supporting Information), therefore, it is expected that if the device switches to the normal state, it will be retrapped to the superconducting state.

As the next step to analyze the dynamics of the induced fluctuations in the NW, we extracted the lifetimes  $t_s$  and  $t_n$  in which the NW is in the superconducting and normal state, respectively. This was implemented by extracting the periods at which the voltage across the device is above and below the threshold at  $0.1\text{ V}$  (see Fig. 3b). Figure 3d shows the distribution of the current-dependent lifetimes  $t_s$  (blue color) and  $t_n$  (red color) at  $V_{sg} = 5\text{ V}$  and  $I = 4.2\ \mu\text{A}$ . The black-dashed curve in Fig. 3d is the fitting of the  $t_s$  histogram (blue histogram) with an exponential,  $n = (1/t_{sd}) \exp(-t/t_{sd})$  with  $t_{sd}$  as fitting parameter. The fitting shows that the distribution follows an exponential dependence (See also the Supporting Information). The same fitting was implemented for both distributions, for the bias current values in the interval indicated by the red dashed lines in Fig. 3a. The inset of Fig. 3d presents the extracted decay times  $t_{sd}$  and  $t_{nd}$  (blue and red circles) and the average lifetimes  $\langle t_{s/n} \rangle$  (blue and red curves) for both distributions as a function of the bias current. The nice matching between the two quantities for both lifetimes indicates that the switching of the NW under the influence of the gate in this region resembles the Poisson process<sup>35</sup>. Furthermore, as the bias current is increased, the lifetime of the NW in the normal state is increased, while it stays for a shorter time in the superconducting state. On the other hand, the distribution of the lifetimes indicates that the gate-induced fluctuations in the NW are slow and can have long time scales.

The analysis of the time-domain measurements for the voltage across the NW at  $V_{sg} = 5\text{ V}$  shows well-defined two-level fluctuations between the superconducting and normal states. However, at higher gate voltages, we noticed that the fluctuations of the system were different. Figure 3e presents the time-average  $V-I$  curve measured at  $V_{sg} = 5.35\text{ V}$ . Even though the ramp rate of the bias current is very slow ( $0.336\text{ nA/s}$ ), we observed that the time-average of the voltage has almost a constant value where the bias current was increased from  $2.4\ \mu\text{A}$  up to  $3.28\ \mu\text{A}$  (the bias current interval indicated by the two red dashed lines in Fig. 3e) compared to the same interval in the  $V-I$  curve



**Fig. 2 | Noise correlation measurements.** **a** The  $V - I$  characteristics of the NW device are measured simultaneously with the noise measurements at  $V_{sg} = 5$  V. **b** The noise spectrum of the NW device at different bias current values is pointed out by the colored arrows in panel **a**. **c** The Coherence,  $C_V$  between the leakage current noise and the NW noise spectra presented in panel **b**. Every single point

represents an average for one octave in  $f$ . The colors correspond to the current value where they are measured. **d** Time traces for the fluctuations on top of the leakage current (gray time trace) at  $V_{sg} = 5$  V and the voltage fluctuations across the NW device (red time trace) at  $I = 5.3$   $\mu$ A.

measured at  $V_{sg} = 5$  V shown in Fig. 3a. The time trace of the voltage at  $I = 3$   $\mu$ A is plotted in Fig. 3f, which shows that the system fluctuates between the superconducting state (red circle) and a wide range of different finite voltage values (blue arrow). This can also be observed from the normalized distribution (yellow distribution) of these voltage states shown in Fig. 3g. Since the finite-voltage state is not at the same level as the normal-state voltage, we will denote it as the intermediate-voltage state. Figure 3h shows the average voltage of the intermediate state ( $V_{int}$ ) as a function of the bias current in the interval indicated by the two red dashed lines in Fig. 3e. The resistance obtained from fitting the curve with a linear function is  $R_{int} \approx 10.4$   $\Omega$ , which is significantly lower than that of the normal state. As the bias current increases beyond this regime, e.g., at  $I = 3.8$   $\mu$ A, the distribution (green distribution in Fig. 3g) shows that the system fluctuates between a low-voltage state and the normal state (see also the Supporting Information). These fluctuations resemble those observed at  $V_{sg} = 5$  V, i.e., Fig. 3c (having a resistance of 80  $\Omega$ ).

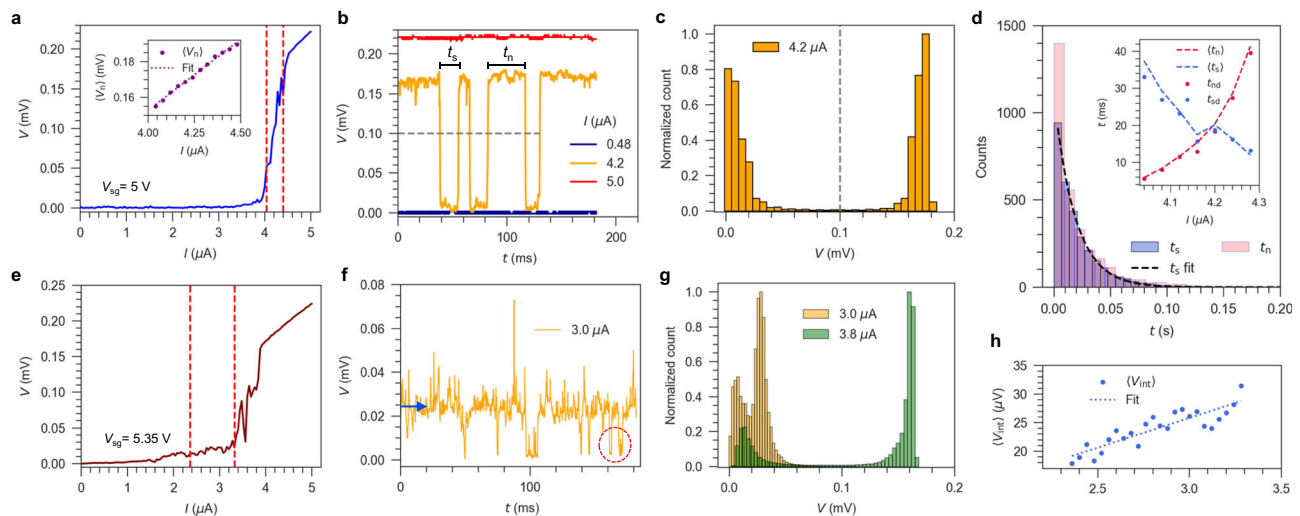
## Discussion

In order to understand the origin of the  $1/f^\alpha$  noise in the leakage current, we should emphasize that the gate dependence of the device has been investigated in two different cooldowns. In the first cooldown, the switching current of the NW device was fully suppressed at  $\pm 15$  V applied on the gate (see the Supporting Information) after initial training measurements<sup>21</sup>. In the second cooldown, this gate voltage window where  $I_{SW}$  is fully suppressed has been reduced to  $\pm 6$  V (see Fig. 1b) after initial training. Figure 4a presents the  $I_{leak}$  as a function of  $V_{sg}$  in both cooldowns. The figure shows the leakage current is significantly increased at lower gate voltages in the second cooldown, similar to the trend observed during the initial training as well<sup>21</sup>. The enhancement of leakage current after applying a higher gate voltage is

consistent with the stress-induced leakage current (SILC) that was observed in gate oxides of the MOSFET transistors<sup>36–38</sup>.

Based on ref. 37, when a high voltage is applied across the gate oxide in the Fowler-Nordheim regime (see Fig. 4c), the high-energy electrons, which tunnel through the oxide potential barrier, suffer collisions with the atoms of the oxide, resulting in damage and hence creating charge traps in the oxide layer. These charge traps serve as intermediate sites, which can increase the leakage current at lower applied voltages via trap-assisted tunneling. In the case of thick oxides, as in our case (the oxide layer between the gate and the NW), multiple traps are assumed to assist in the conduction process<sup>39,40</sup>. The generated charge traps can trap electrons and randomly release them with long time constants giving rise to fluctuations in the trap-assisted tunneling and hence the presence of  $1/f^\alpha$  noise in the  $I_{SILC}$ <sup>38,41</sup>. These time scales are consistent with the time scales of fluctuations observed in our case (see Fig. 3d). Furthermore, a characteristic property of SILC is that the normalized current noise  $S_I/I_{SILC}^2$  should be independent of the applied gate voltages<sup>38</sup>. Figure 4b shows the  $S_I/I_{leak}^2$  as a function of  $V_{sg}$  at  $f = 10$  Hz in the gate voltage window at which  $I_{SW}$  is suppressed. The ratio  $S_I/I_{leak}^2$  is constant with increasing  $V_{sg}$  as expected for SILC process<sup>38</sup>. Furthermore, the dominant conduction mechanism in the SILC is inelastic tunneling<sup>42</sup>, in which electron energy relaxation takes place predominantly with the emission of phonons (see Fig. 4d)<sup>43,44</sup>. In our case, the emitted phonons can propagate through the substrate, couple with the superconducting NW, and cause the GCS effect<sup>22</sup>. In addition, this energy relaxation could also excite surface plasmons, and their decay with photon generation can also contribute to GCS<sup>45</sup>.

Considering the time-domain measurements at 5.35 V, the appearance of an intermediate-voltage state (see Fig. 3f) with a resistance of  $R_{int} = 10.4$   $\Omega \ll R_n$  is consistent with a short segment of the NW having been switched to the normal state (see Fig. 4e). As  $V_{sg}$  is



**Fig. 3 | Analysis of the time-domain measurements.** **a** The  $V-I$  curve of the NW device measured at  $V_{\text{sg}} = 5$  V. The inset shows the average high-voltage state  $\langle V_n \rangle$  as a function of the bias current in the interval surrounded by the two red dashed lines in panel **a**. The high-voltage state  $\langle V_n \rangle$  is obtained by extracting and averaging the voltage above the threshold at  $V = 0.1$  V indicated by the gray dashed lines in panels **b** and **c**. The dashed line is the linear fitting of  $\langle V_n \rangle$  with a corresponding resistance of  $R \approx 80 \Omega$ . **b** Representative segments from time traces of the voltage across the NW,  $V$ , at different bias current values.  $t_s$  and  $t_n$  represent the lifetimes at which the superconducting NW is in superconducting and normal state, respectively. **c** The probability distribution of the measured voltages along the time traces at  $I = 4.2 \mu\text{A}$ . **d** The distribution of the lifetimes of the high-voltage state  $t_n$  (red distribution) and the low-voltage state  $t_s$  (blue distribution) extracted from time traces at  $V_{\text{sg}} = 5$  V and  $I = 4.2 \mu\text{A}$ . The black dashed curve is a fitting of the probability

distribution of the  $t_s$  histogram (blue) with an exponential  $n = (1/t_{\text{sd}}) \exp(-t/t_{\text{sd}})$ . The inset shows the decay times  $t_{\text{sd}}$  and  $t_{\text{nd}}$  (blue and red circles) extracted from the fitting of  $t_s$  and  $t_n$  distributions and the average lifetimes  $\langle t_{s/n} \rangle$  (blue and red curves) of the two distributions as a function of the bias current. **e** The time average of the  $V-I$  curve of the NW device at  $V_{\text{sg}} = 5.35$  V. **f** A segment of the time trace of the voltage across the NW,  $V$ , at  $I = 3 \mu\text{A}$ . The time trace exhibits two different voltage states: a low-voltage state (red circle) and an intermediate-voltage state (blue arrow). **g** The normalized distribution of the measured voltages along the time traces was measured at  $I = 3 \mu\text{A}$  and at  $I = 3.8 \mu\text{A}$ . **h** The average intermediate-voltage state  $\langle V_{\text{int}} \rangle$  as a function of the bias current in the interval surrounded by the two red dashed lines in panel **e**. The dashed line is the linear fitting of  $\langle V_{\text{int}} \rangle$  with a corresponding resistance of  $R \approx 10 \Omega$ .

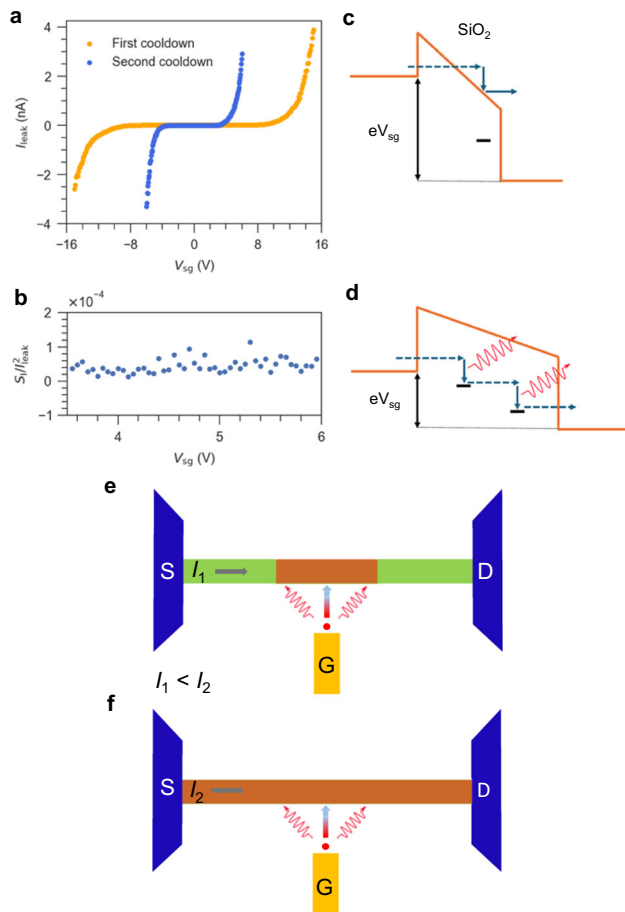
increased, the leakage current reaches a threshold at which the electrons or the generated phonons can induce phase slips in the superconductor NW at the position where most of the energy is transferred (see orange region)<sup>46,47</sup>. Since the bias current is small, the heat dissipated by the phase slip is not enough to switch the whole superconducting NW to its normal state; thus, other sections (green regions) remain superconducting. The ratio  $R_{\text{int}}/R_n$  indicates that the NW segment that switched to the normal state has a length of  $L_n \approx 160$  nm, which is consistent with the minimal size of a phase slip center, which has a value of  $2\xi \approx 156$  nm (see Methods)<sup>48</sup>, where  $\xi$  is the superconducting coherence length in the Al shell. However, the leakage current has a strong fluctuation around its main value (see Fig. 2d), as a result, the phonon-mediated heat transfer also varies, resulting in a fluctuation in the size of the normal segment and the scattering in the value of  $V_{\text{int}}$  (see Fig. 3f). We also emphasize that at this gate voltage regime, the switching of the NW to the normal state due to macroscopic quantum tunneling and thermally activated phase slips is negligible compared to the gate-induced phase slips as reported in refs. 9,23.

As the bias current is increased, the heat dissipated by the induced phase slips becomes sufficient to switch the whole NW to the normal state (see Fig. 4f). Since  $I_{\text{SW}}$  and  $I_r$  are almost equal at this gate voltage regime (see the Supporting Information), the NW gets retrapped again to the superconducting state when the fluctuating leakage current gets reduced (see Fig. 2d). As a consequence, the voltage across the NW fluctuates between two discrete states (Fig. 3c), which induces a Lorentzian spectrum in the power spectral density (see Fig. 2b). With further increases in the bias current, the heat dissipated by the phase slips will be enough to switch the entire wire and keep it in its normal state.

The measurements at two different gate voltages are consistent with this picture since at lower gate voltages (e.g., at  $V_{\text{sg}} = 5$  V), the induced voltage fluctuations appear at larger bias current values, where the Joule heating in the phase slip center switches the whole NW

to the normal state and it retraps back to the superconducting state. At large gate voltages (e.g., at  $V_{\text{sg}} = 5.35$  V), the gate-induced fluctuations are increased such that they can induce voltage fluctuations already at low bias current values, but this is only enough to switch a short segment of the NW to the normal state, which results in the appearance of the intermediate voltage state at this elevated gate voltage. At larger bias current values, the two-level fluctuation also shows up, where the NW fluctuates between entire superconducting and normal states.

In this work, we characterized the GCS effect in Al/InAs NW-based devices by  $1/f^\alpha$  noise measurements. The noise correlation measurements show a large correlation between the leakage current noise and the induced voltage noise in the superconducting NW. Our findings suggest that the GCS effect originated from phonons generated by inelastic tunneling of the electrons through the trap states created by stressing the oxide layer between the gate and the NW under a high electric field, which is qualitatively consistent with the microscopic picture proposed by ref. 22. Moreover, our results show that even an individual resistance fluctuator can control the switching of the supercurrent in the nanowire. This is an important finding, which means that even a very small change in the inelastic tunneling current at a critical spot can lead to abrupt switching of the supercurrent. Identification of such a critical spot would make these systems very promising elements for fast superconducting electronics. These spots are likely in close contact with the nanowire, where the influence of the generated phonons is maximized. Furthermore, besides phonon emission in inelastic tunneling, there should also be photon emission, which could also contribute to the switching of the superconductor. Such photons could be directly verified using low-temperature optical emission experiments. Considering superconducting gating for fast logic circuits, the speed of switching back to the superconducting state is expected to be the limiting factor since it is governed by thermal processes and their intrinsic speed. With Al superconductor below 1 K the thermal response speeds are limited to frequencies  $f \leq 1$  GHz owing



**Fig. 4 | Interpretation of the dynamics of the GCS effect.** **a**  $I_{\text{leak}}$  as a function of  $V_{\text{sg}}$  of the NW device in two different cooldowns. **b** Normalized current noise  $S_I/I_{\text{leak}}^2$  as a function of  $V_{\text{sg}}$  at  $f = 10$  Hz, which is consistent with resistance fluctuations. **c** Schematics of generation of the charge traps (black horizontal line) in the oxide layer by the collision of high-energy electrons with the atoms of the oxide<sup>37</sup>. **d** Multiple trap-assisted tunneling. The inelastic tunneling of electrons through the trap states is associated with phonons emission (red arrows). **e** Schematics of the switching mechanism of the superconducting NW (SC) to the normal state (N) by the phonons (red arrows) generated by the inelastic tunneling of electrons (red circle) in the case of low bias current values and **(f)** high bias current values. For low bias current, only a short segment of the wire switches to normal (the orange part), while for large current, the dissipation in the short segment is enough to bring the entire wire to normal.

to low superconducting transition temperature. However, by using materials with large critical temperatures such as NbTiN<sup>49</sup>, much larger thermal speeds could be achieved. Presuming that the operation temperature can be increased from -1 to 5 K, electronic thermal cooling will be replaced by electron-phonon heat transfer<sup>50</sup>, and the operation speed can be increased by two orders of magnitude, which is suitable for the implementation of fast logic gates. Furthermore, the GCS effect can be useful in various quantum circuits as a fast gate tunable superconducting-normal switch. This could find application e.g., in SQUID-based CPR measurements<sup>51</sup> to switch off the reference junction, or such a unit can be used as a heat switch as well.

## Methods

The devices were fabricated by depositing InAs NWs with a 20-nm-thick full Al shell layer (green)<sup>52</sup> on an undoped Si wafer with a 290-nm-thick oxide layer. After NWs deposition, four Ti/Al contacts (blue) with a thickness of 10/80 nm and two opposite side gates (yellow) made of Ti/Au with a thickness of 7/33 nm were fabricated in two separate

electron beam lithography (EBL) steps. For the device shown in Fig. 1a, the separation between the Al contacts is  $\approx 870$  nm. The distance between the upper gate electrode and the NW is  $\approx 50$  nm, while for the lower gate electrode, it is  $\approx 70$  nm. All the GCS-based measurements on this particular device were performed by applying a voltage  $V_{\text{sg}}$  to the upper gate electrode.

The  $V - I$  characteristics of the device were measured using a quasi-4-probe method in which the current is ramped linearly from negative to positive values by an engineered voltage signal generated by an arbitrary wave function generator (KEYSIGHT 33600A) with a series resistor of 50 k $\Omega$ , while the voltage across the device is measured with a differential low-noise voltage amplifier and a Zürich instruments (UHF-LI 600 MHz) used as an oscilloscope. The ramping rate of the bias current can be controlled by adjusting the sampling frequency of the waveform generator.

The leakage current noise and the voltage noise in the NW device were probed by measuring the noise signals at the gate resistor  $R_G$  and the NW device, respectively. The noise signals were measured by a 2-channel spectrum analyzer (HP89410A). The obtained noise spectra were averaged 20 times. The cross-spectrum and the coherence between the two signals were calculated internally by the spectrum analyzer.

The high-resolution time traces for the voltage fluctuations in the NW device were measured by the quasi-4-probe measurements, whereas the bias current is kept fixed and the voltage across the device is measured as a function of time by the Zürich instruments. On the other hand, the time traces in which both the two signals (leakage current and NW fluctuations) were measured simultaneously were probed by a multi-channel oscilloscope (Tektronix TDS 2014B).

The coherence  $C_{IV}$  between two signals  $X_I(t)$  and  $Y_V(t)$  is defined at a given frequency  $f$  as follows:<sup>53</sup>

$$C_{IV}(f) = \frac{|S_{IV}(f)|^2}{S_I(f)S_V(f)}, \quad (1)$$

where,

$$S_{IV}(f) = \int_{-\infty}^{\infty} E[X_I(t)Y_V(t + \tau_l)] e^{-i2\pi f \tau_l} d\tau_l. \quad (2)$$

is the cross-spectrum between the two signals,  $\tau_l$  is the time delay between the two signals,  $E$  denotes the expectation value.  $S_I$  and  $S_V$  are the corresponding power spectral densities of the two signals.  $C_{IV}$  takes values between 0 and 1, and if the value of the coherence is close to 1, the two signals are strongly correlated. Conversely, the two signals are uncorrelated if the value of the coherence is close to 0<sup>53</sup>.

The coherence length  $\xi$  was calculated by using  $\xi = \sqrt{\hbar l / R_n w t N_f e^2 \Delta_0}$ , where  $l = 870$  nm,  $w = 100$  nm and  $t = 20$  nm are the length, width, and thickness of the NW device, respectively,  $N_f = 2.15 \cdot 10^{47} \text{ J}^{-1} \text{ m}^{-3}$  is the density of states at Fermi level, and  $\Delta_0 = 1.76 k_B T_c$ ,  $T_c = 1$  K.

## Data availability

The data obtained in this study are available in numerical form at: <https://zenodo.org/records/11004848>. Time domain data is available upon request.

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## Author contributions

T.E. and M.B. fabricated the devices, T.E., I.L., and A.S. performed the measurements T.E., M.B., G.F., and L. K. did the data analysis. T.K. and J.N. developed the nanowires. All authors discussed the results and worked on the manuscript. P.M., P.H., and S.C. guided the project.

## Competing interests

The authors declare no competing interests.

## Additional information

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