Increasing Productivity in Vapour Phase Soldering Using Vertical Stacking of Boards

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***Abstract*— During vapour phase soldering, the lateral size of the specimen tray determines the number of assemblies that can be soldered at once. Increased productivity, thus less power consumption can be achieved by increasing the size of the tray, and the workspace of the oven; therefore, also the size of the machine. This means significant additional costs both in terms of machine design and the amount of heat transfer fluid used. The aim of our research was to find out how we can increase the productivity of an industrial grade oven and improve the technology for a more energy efficient production, without making any significant retrofitting modifications. By stacking multiple printed circuit boards (PCB), we could increase the number of PCBs that could be soldered at once up to three times. We designed a sample holder with reduced mass, which shortened the cycle time. We performed comparative tests in several vertical configurations, compared to the default setup. We examined the resulting thermal profiles, performed shear tests, examined the surface of the cracks with optical microscopy, and also performed a cross section analysis. The results show that the solder joint quality was degraded due to increased void formation; however, the overall product quality might fit the requirements of commercial electronics.**

Keywords— vapour phase soldering, reflow, sustainable manufacturing, productivity

I. Introduction

Reflow soldering is an essential step in electronics manufacturing technology [1]. Vapour phase soldering (VPS) [2] is becoming increasingly popular and there are some cases where it may be the only effective method for obtaining joints with acceptable quality. For example, temperature-sensitive components can only be soldered safely using this method, while the peak temperature is maximised by the boiling point of the heat transfer fluid (Galden [3]) and the mode of operation, which results in a much more uniform heat distribution over the surface of the substrate. Also, for large, power electronics components, VPS can be a choice for quality results, due to the reasons mentioned above. In the current VPS technology, the control of vapour phase soldering equipment is based on temperature [4]. Measuring the temperature of the vapour space is hardly trivial, since the most fundamental problem is that the measured value depends on the parameters of the thermometer placed in the vapour space.

Vapour is heavier than air, so this vapour accumulates on top of the liquid, filling the bottom of the tank, forming a vapour blanket. During the process, the PCB with the paste and component is placed in this vapour space. Here the temperature difference (sudden entrance of a colder PCB) causes condensation, resulting in heat transfer. The advantage of this method of soldering is that the temperature cannot exceed the boiling point.

The disadvantage of this method is that it is more difficult to integrate into a production line. The high cost of the heat transfer medium is also a limiting factor of application. Some components, typically open gas sensors, or specific packages cannot be soldered in such equipment, because the liquid can damage them.

However, smaller size equipment can be perfect for prototyping companies.

II. The possibility of stacked Soldering

There are several methods for reflow soldering. The hot air or inert gas heat transfer method [5] is one of the most common tunnel furnaces in industry, it is unsuitable for soldering stacked PCBs. The PCBs on top provide a mask for the substrates below, so there will be poor heat transfer in the bottom-up layers. In the case where the heat transfer is directed from the side, the gas will arrive parallel to the PCB surface and heat transfer will not be proper considering the flow regimes at the total surface area of the PCB. If we consider infrared furnaces [5], we can also encounter the same problem of masking, only the top (or bottom) panels will have proper heat transfer.

With vapour phase soldering, these problems do not occur, because the vapour space surrounds the substrates from all directions. There is also a continuous flow of energy between the layers, as the condensing vapour turns into a liquid and the generated gradient (loss of vapour) in the vapour space draws more vapour around the solderable specimen. We can see that in vapour phase equipment, it is theoretically possible to perform stack soldering, but there are some limitations to consider.

The most basic physical limitation of such an equipment (e.g. our apparatus, the later presented Asscon VP 800) is that the height of the front-loading opening is limited. No stack higher than this can be placed on the tray. We know from our previous research that there is a vapour space of 8-10 cm above the tray [5], so theoretically this is the maximum stack height that can be

built. Since the upper layers of the vapour space are unsaturated with an increasing gradient upwards, it is assumed that only a smaller stack can be soldered.

In this paper, we aim to investigate this aspect of vapour phase soldering and try to define the limits of stacking in terms of methodology and final quality of the joints, in an industrial grade VPS reflow oven.

III. Experimental, Initial Tests

During the first measurement, we performed paste melting tests on two different stack layouts (Figure 1). We used the aforementioned Asscon VP800 vapour phase soldering oven, which is capable of controlled heat-level-based soldering. This means, that the PCB is lowered into the vapour space, and then vapour is generated onto the surface of the boards.

We placed SAC305 (Senju, M705 [Sn96.5-Ag3.0-Cu0.5]) paste on the surface of the PCBs and arranged them in stacks.

In all cases, the stack starts with a bolt head from the bottom up, which secures the spacer to the bottom substrate. The height of the screw head is 2 mm. The thickness of the panels is 1.6 mm. (Standard FR4-based PCBs.)

In the first test we assembled a stack of five PCBs using a 20 mm spacer. In this case, the paste melted on the bottom three PCB surfaces and dried completely on the others. As a result, we found that the soldering height limit was between 47 and 67 mm. We then refined the stack and prepared a stack of six PCBs, but this time using a 10 mm height spacer. In this configuration the solder melted on the bottom five PCBs. From this result we concluded that the limit was between 50-60 mm.

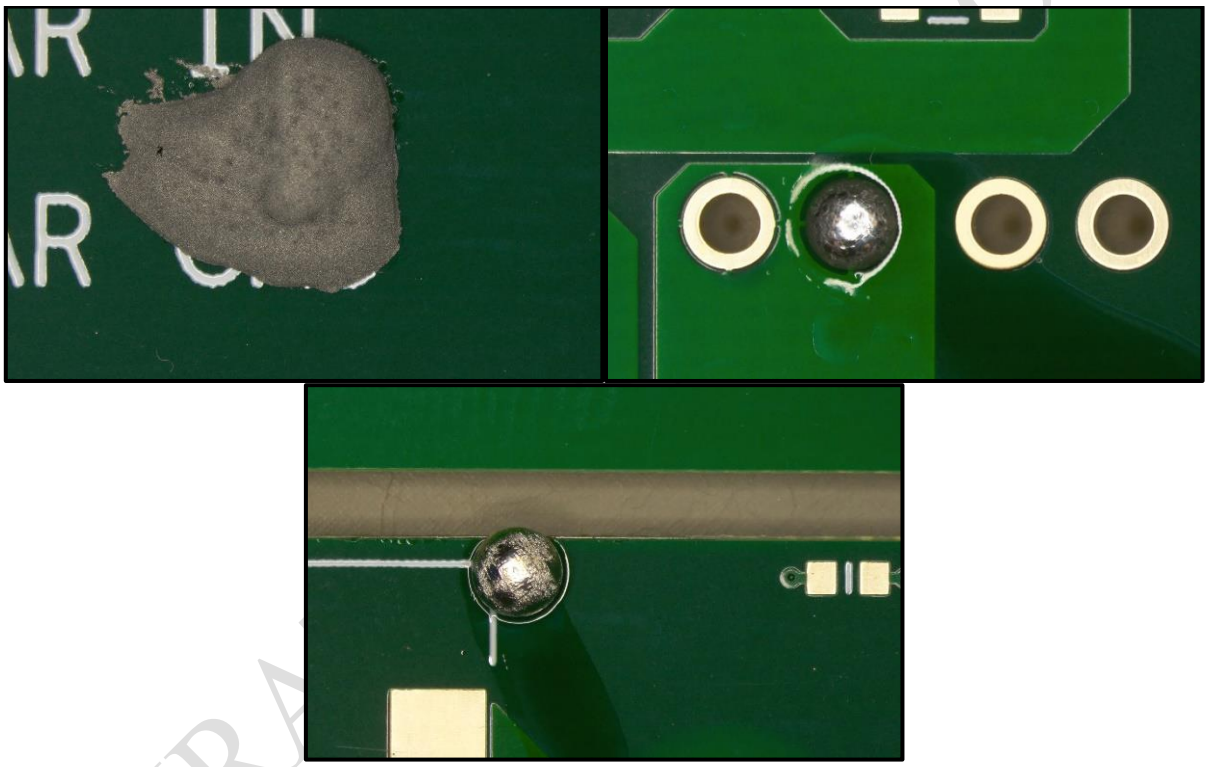
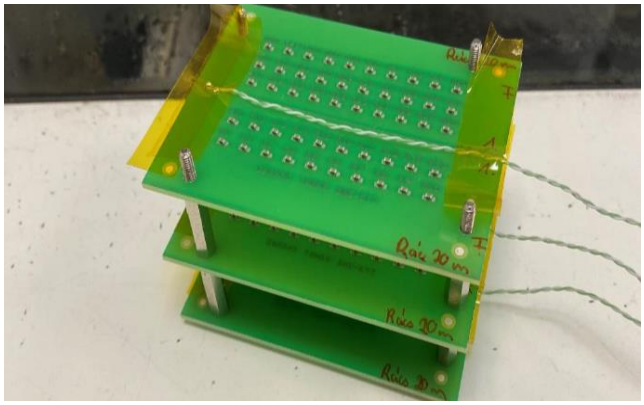


Fig. 1. Bottom picture: PCB 1, Middle picture: PCB 5. Top picture: PCB 6, where the paste has not melted.

The boundary is out of the focus, while uncertain results are not acceptable in actual production. We therefore continued with a value lower than the specified limit; we used a stack of 3 PCBs using a 20 mm spacer. Thus, the total height of the stack is 47 mm. The final stack layout is shown in Figure 2.



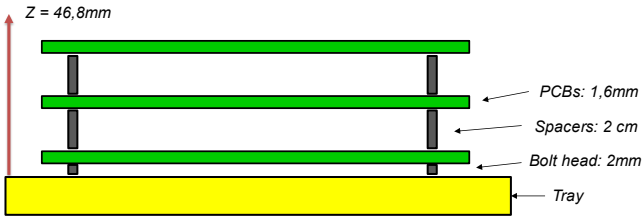


Fig. 2. The final stack layout.

The VP800 oven includes a solid aluminium tray with a weight of 4.4 kg. This was designed to be used with a vacuum unit, which is lowered onto the tray in the form of a flange at the end of the soldering cycle to reduce the formation of voids. This step requires a solid tray, as this is the only way to create a vacuum. The VP800 unit is also working without a vacuum unit, so we decided to experiment with the basic program, without the vacuum step at the end.

The system requires considerable heat to heat the tray. Therefore, we have designed a reduced tray made of an aluminium frame and an aluminium grid. The installation of the resulting grid is shown in the figure, with a mass of 0.76 kg. Also, the new tray enables better vapour flow from the bottom of the stack.

Fig. 3. The built-in reduced tray (grid-based)

We worked with both trays, to find the effect of this considerable thermal capacitance inside the system. The sets of experiments were carried out on different days, in order to start with a cooled oven in each case.

First part of the tests was performed with the factory tray:

- Factory tray: first soldering: 1 PCB
- Factory tray: first stack soldering: 3 PCB
- Factory tray: second soldering: 1 PCB
- Factory tray: second stack soldering: 3 PCB

The tray was then replaced with the retrofitted reduced tray, where measurements were taken using the same order:

- Reduced tray: first soldering: 1 PCB
- Reduced tray: first stack soldering: 3 PCB
- Reduced tray: second soldering: 1 PCB
- Reduced tray: second stack soldering: 3 PCB

During the measurements, we continuously saved a heat profile using the V-Mole (ECD, USA) tool with K-type thermocouples (±1°C accuracy, TC Direct, UK). After soldering, we performed a shear test on 30 components. On the PCB, 50 pieces of capacitors were soldered. It is important to note that it is not practical to place the V-Mole device in a vapour space, so for all measurements the device was positioned outside the equipment, at a sufficient distance from the work area to isolate the cold junction reference; the thermocouple wires were routed through the door of the equipment into the work area.

In each arrangement, we therefore performed the same measurement twice. The results do not differ between the two, and only one of the two measurements will be presented in the following.

The heating factor (1) shows the area under the curve above the melting temperature. This is used later in evaluating the profiles. It is proportional to the TAL times, considering that the solder paste always melts at 217 °C and the Galden vapour temperature is always 240 °C in our setups.

$$Q\eta = \int_{t0}^{tc} (T(t) - T_0)\ dt \qquad (1)$$

where Qη is the heating factor [sK], T(t) is the temperature to saturation [°C], T_0 is the melting point of the solder, see above [°C]; t_0 to t_c is the window of TAL (time above liquid) [sec].

The shear tests were carried out with a DAGE BT 2400 shear tester. In this device, the shear tester knife locates the surface of the substrate and continuously pushes the component against the knife at a set height relative to it. A force is then generated between the contacting surfaces, which is continuously locked by the device. This force increases continuously until a break occurs. The highest value from the recorded force diagram gives the breaking force.

IV. Results – Heat profiles

A. *Golden sample: (Factory tray + 1 PCB)*

The equipment was operated with the factory heat profile setting. The two temperature spikes on the front of the heat profile are due to the two-step movement of the tray. At the first stop, the tray absorbs the energy of the vapour space, which is thus dissipated, but there is still vapour under the tray. On the second movement, the tray enters the remaining vapour, from which it takes the remaining energy, causing the second spike.

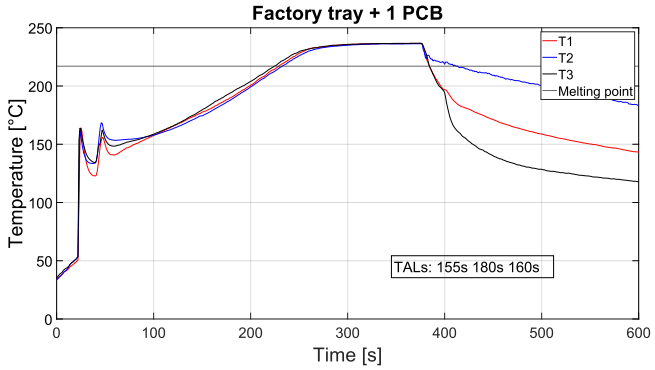


Fig. 4. Heat profile of the golden sample

The actual soldering cycle then begins when the heating plates reheat the vapour space. The time spent in the liquid state (TAL: time above liquid) is around 160-180 seconds, with heating occurring at a rate of 0.45 K/s. The total cycle time is 606 seconds. The separation of the three signals shown at the end is a negligible measurement error, the thermocouples were fixed to the substrate with Kapton tape, which slipped out of the adhesive due to the movement of the wires during the lift up.

B. *Factory tray + 3 PCB stack:*

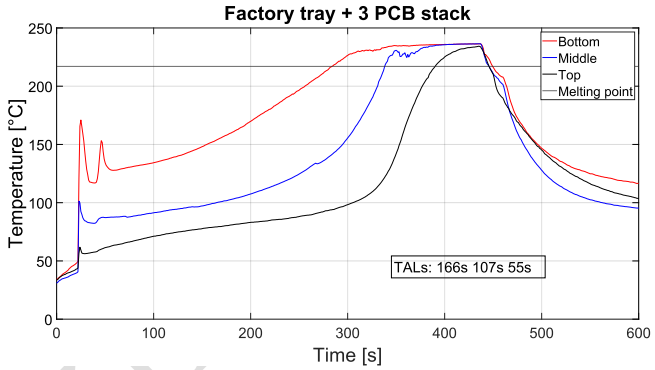


Fig. 5. Heat profile of the stack, in the factory tray

In this measurement, we also used the factory tray, and we soldered the stack layout as shown earlier. The resulting heat profile is shown in Figure 5. The double spike resulting from the tray movement is only present at the beginning of the profile for the bottom substrate, minimal at the middle and disappears completely at the top. This shows that there is weaker heat transfer between the vapour and the substrate at these levels. Over time, the vapour layer gradually rebuilds, resulting in a shift between the different levels. It can be seen that the upper heat profile spends significantly less time (55 s) above the melting point (TAL) than in the first case (166 s).

The rate of heating also varies, with the bottom panel being the slowest (0.4 K/s) which is the same as the flat soldering, while the middle and top panels heat at 1.5 and 1.7 K/s respectively. Here the total cycle time is slightly longer at 667 seconds.

C. *Reduced tray + 1 PCB:*

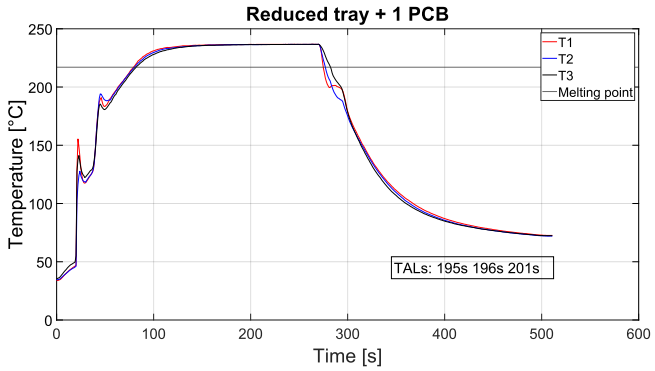


Fig. 6 Heat profile of one PCB in the self-made grid

We then replaced the tray with the reduced grid. This was done in cold condition so that the same measurements were taken in the same order for both the tray and the grid. By using the grid, significantly less mass is placed in the vapour space and therefore the substrate temperature can increase at a much higher rate. The spikes have changed, with the substrate temperature reaching 190 °C during the second movement. At around 120 seconds the substrate reaches the Galden boiling point of 240 °C. A change of 210 °C occurs in 120 seconds. The TAL increases to around 200 seconds.

D. *Reduced tray + 3 PCB stack:*

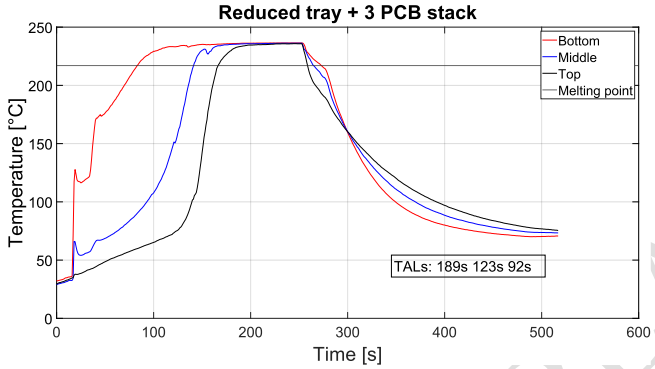


Fig. 7. Heat profile of the stack in the self-made grid

In the last case, stack soldering was performed on the grid, the heat profile of which is shown in Figure 15. Here again we see a delay between the different levels due to the different heights.

E. *Summary*

The summarized results of the heat profiles are shown in Table 1. Using the factory soldering setup as a starting point, the stack on the tray has a higher heating rate and in parallel the TAL times decrease. We see a similar trend for the reduced tray, but here we see a 10x increase in temperature rise in the worst case.

The cycle time is reduced when the reduced grid is used, which is to be expected, due to the mass reduction shown earlier; the energy saved here is also reflected in the time taken to heat the tray.

V. Results – Shear Force

During the shear tests, the rupture occurred between the solder meniscus and the PCB pad. A common problem in shear tests is that the fracture does not occur in the solder joint but in the component's termination or at the lifting of the pad. This was not the case here, so the results are considered to be valid. Figure 8 shows the shearing tool before testing.

TABLE I. – STACK TYPES / RECORDED PARAMETERS

	TAL [s]	**Speed [K/s]**	**Cycle time [s]**	**Heating factor [sK]**
Tray, no stack	160	0,45	606	2480
Tray stack – bottom	166	0,41	667	2505
Tray stack – middle	106	1,54	667	1595
Tray stack – top	55	1,7	667	650

Grid, no stack	200	1,75	500	3400
Grid – bottom	189	2,31	483	3044
Grid – middle	123	3	483	2019
Grid – top	92	4	483	1455

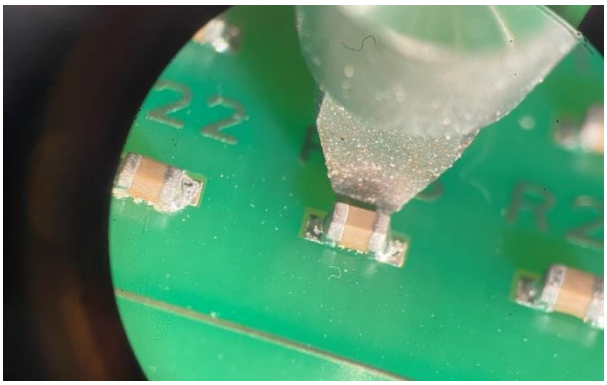


Fig. 8. Shear tester: knife positioned at the side of the component

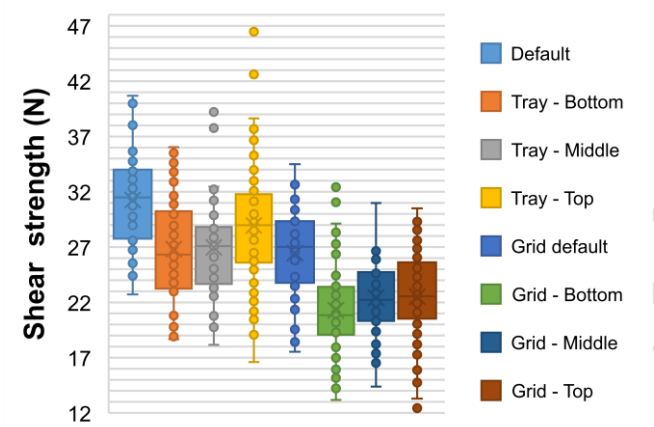


Fig. 9. Shear strength results

Soldering with the original factory profile gave the best results. In comparison, there is a quality decrease when soldering with stack. Here the degradation within the stack is almost uniform across the three levels.

Further degradation was observed when soldering with the reduced grid-based tray. The worst result was stack soldering on the grid. Again, we got almost identical values within the stack.

The properties of the factory heat profile are quite different from those of the soldered-on grid stack. Compared to the factory profile slow heating rate, the steepest part of the solder joint can reach 4.7 K/s. Within the stack, there is no significant difference in the break down values even though the TAL is significantly different at the different configurations.

The standard deviation and spread are consistent across the tests, with only a few outliers in our work.

So, it can be said that the degradation of the solder joint quality may be related to the increase of the heating rate, which may lead to a degradation of the wetting, and it may cause more voids in solder joint.

It is also worth making a literature comparison with the quality of the solder joints at this point. For 0603 resistors, the following table (II.) summarises the general shear strengths:

TABLE II.

LITERATURE	AVERAGE [N]	MIN [N]	MAX [N]
[6]	18	14	24
[7]	~30	24	41
[8]	25	22	30
[9]	32	-	-
CURRENT RESULT	21-31	12-23	30-41

The results of the table show that our own results, which can be considered worse, show similar values compared to the literature values, so stack soldering may be applicable in certain cases (within given quality limits, for example for commercial use).

VI. Results – Cross section analysis

Since there were significant differences in the shear forces, and the analysis of the heat profiles alone do not provide a satisfactory explanation of the behaviour, it was considered necessary to investigate the soldered joints by cross-sectional images. During sample preparation, the part to be tested is removed from the substrate and embedded in epoxy resin. After hardening, the sample undergoes a multi-step grinding and polishing process. It is then possible to examine the solder joint along the cross-section of the sample using an optical microscope. From the parts left on the test panels, 3 parts could be included in a sample. we did not consider it necessary to examine the entire sample, as the extreme values and an intermediate value can provide sufficient information.

In total, four samples were taken:

- one of the soldering from golden sample, where the sample was made with the factory tray without stack (best)
- one of the stack on the grid (worst)
- one from a non-stack soldering on the grid (intermediate)
- one from a stack on the tray (intermediate)

Picture of the "golden" sample made in the factory tray is shown in Figure 10. The solder cross-section is nearly uniform and homogeneous. Determining the thickness of the intermetallic layer in this way is very difficult, but by visual inspection, "averaging", it can be said to be in the range of a few microns.

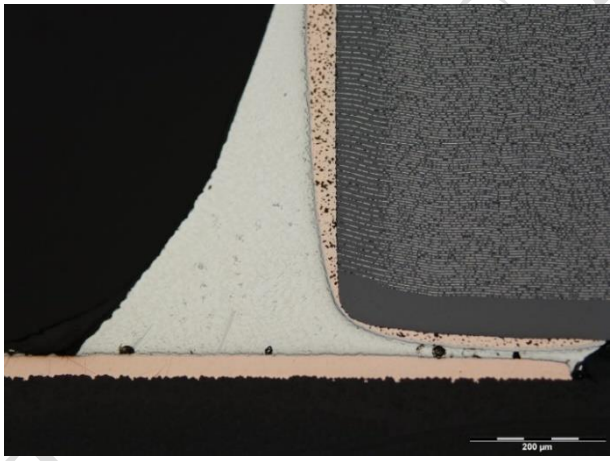


Fig. 10. Golden sample: factory tray + 1 PCB

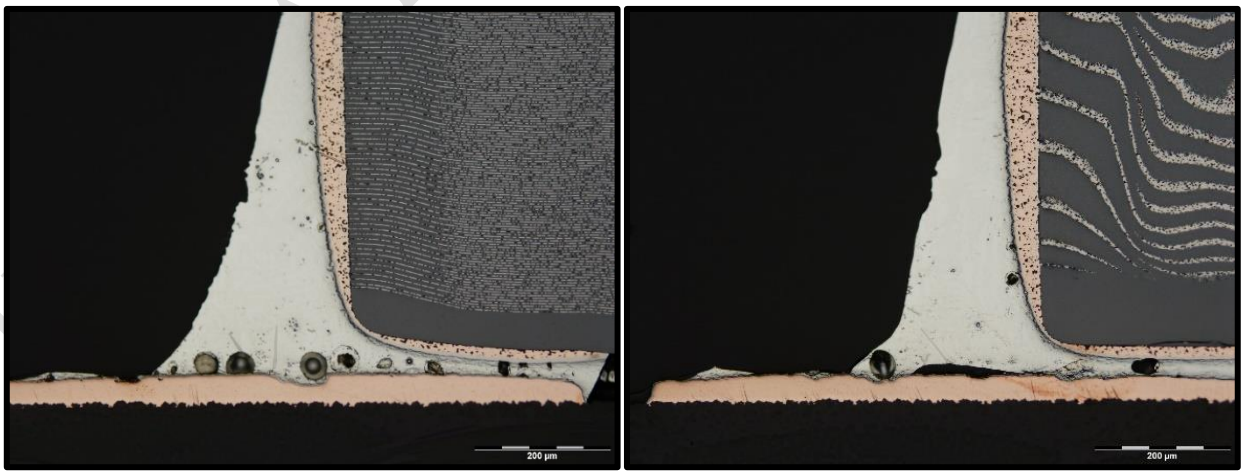


Fig. 11. Two sample from the reduced tray

Figure 11 shows cross section images of the middle panel of the grid stack. The formation of the meniscus is not perfect, which may indicate a wetting problem. The number and size of voids is also significant.

In the factory soldered configuration, only a few insignificant voids were observed. In contrast, the number of voids and their size increased with the reduced grid. In Figure 10 you can see the homogeneity of the solder, in contrast to the increased number and size of voids in Figure 11.

Optical microscopy was also used to examine the surfaces of the component (Figure 12.)

The top picture shows the result of soldering without a stack in factory configuration. The surface of the solder is uniform with a few voids. The picture also shows a part from the middle panel of a stack made on the grid. The surface is not nearly uniform anymore, it has a spongy texture and is covered with voids.

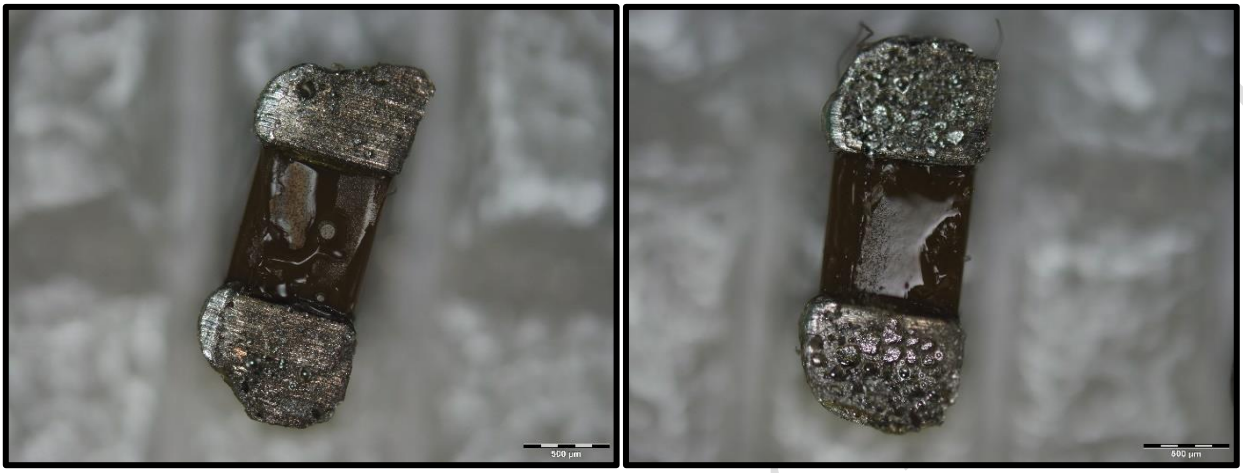


Fig. 12. Top: golden sample, Bottom: reduced grid, stack

As a result, we can say that the change in the shear forces is caused by the more significant formation of voids. The effective load bearing cross-section of a meniscus is significantly reduced because of the voids, so it can withstand lower forces. The excessive void formation can be explained by the modified heat profiles. The average activation temperature of the flux is 125 °C. In contrast, in the modified heat profiles, the substrate spends much of its time below 100 °C, during which only the paste dries. After that, the maximum temperature is reached by a large temperature rise. Thus, the flux cannot perform its function and its remains cannot leave the solder during the shorter cycle time, and the meniscus formation is affected due to poor wetting. This explains our results, further studies are needed to investigate the effect of changing the flux (flux - fluxing agent).

VII. Conclusion

In the paper we investigated the use of a reduced tray and stack-based soldering in an industrial vapour phase soldering oven. It was found that the shear strength of the joints were reduced from the factory-settings (~30 N) to (~27 N) with the inclusion of stacked soldering, and then it was further reduced to (~20 N), when a sampler holder tray with reduced thermal mass was introduced to the system. It means, that the shielding effect of the original tray might be in favour of the overall joint quality. It must be noted that the quality decrease was due to reduced wetting and increased voiding. The technique may be applicable within certain limits (e.g. commercial electronics), while the results are still in line with literature data.

It is important to note that the reduction from 667 seconds to 483 seconds represents a reduction of about 30% in the time operation of the equipment. This does not clearly correlate with the power consumption, but it shows that a non-negligible energy reduction could be achieved at the equipment level with such a modification (grid). In addition, the required power per joint (W/joint) for a triple stack could also be divided by a factor of three, further increasing energy efficiency. Based on the above SDG (Sustainability Development Goal) points [10], our result is linked to point 9 (industry, innovation, and infrastructure) and also to point 12 (responsible consumption and production). In the future, we would like to investigate soldering with a vacuum unit, as voids are the cause of joint degradation. Vacuum may be a solution to this problem. Also, setting in the profiles might enable more efficient, and higher quality joints, with reduced time, to further increase productivity and power reduction.

ACKNOWLEDGEMENT

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