Power Electronics Solar Inverter on a Biosourced and Biodegradable Substrate – Thermal Study

Vincent Grennerat[1,2)], Pascal Xavier[1)], Pierre-Olivier Jeannin[2)], Attila Géczy[3)]

[1)] CROMA, Univ. Grenoble Alpes, Université Savoie Mont-Blanc, CNRS, Grenoble INP, 38000 Grenoble, France

[2)] Univ. Grenoble Alpes, CNRS, Grenoble INP, G2Elab, 38000 Grenoble, France

[3)] Dept. of Electronics Technology, Faculty of Electrical Eng. and Informatics, Budapest Univ. of Technology and Economics

Vincent.Grennerat@univ-grenoble-alpes.fr

Abstract— This paper presents a comparative study between traditional and sustainable approaches on a power electronics inverter; it focuses on the thermal management of the DC-AC bridge thermal losses. The system is based on the design of the DC-AC stage of a commercial photovoltaic inverter, from which an as close as possible design copy was realized on a traditional printed circuit board flame retardant 4 (FR4) substrate, made of 4 copper layers (reference design). An adaptation of this design was prepared to implement it on a novel biobased and biodegradable substrate based on polylactic acid (PLA), flax fibers and biosourced flame retardant, with only 2 copper layers. Because this composite has a reduced glass transition temperature compared to FR4, it makes it more sensitive to intense thermal dissipation. In this system, the thermal dissipation is achieved through the PCB with thermal vias. An analytical modeling was performed to evaluate the thermal resistance of the vias in both designs and the resulting increase of temperature of the substrate. Thermal infrared measurements were then conducted on both designs, at selected operating points to evaluate the possibilities and limitations of the bio-substrate on such application.

Keywords— Sustainable electronics, power electronics, DC-AC inverter, bio-based PCB substrates, thermal management

I. INTRODUCTION

The strong increase of waste from electrical and electronic equipment (WEEE) is the motivation for research studies to make the life cycle of electronic devices sustainable. Reducing the greenhouse gas emissions is one of the targets, but reducing the pressure on non-renewable resources and increasing the possibilities of repair, reuse and recycle of the product are also some important motivations.

New biosourced and/or biodegradable substrates were developed for these purposes during the last years [1], [2], as well as some highly recyclable materials [3], providing alternatives to the traditional Flame Retardant class-4 (FR4) epoxy-resin composites. Although literature does not describe the approach of commercial electronic products, there is an increasing number of significant technological prototypes which were made with these environmentally friendly substrates [4].

The 2050 net-zero carbon target has started to shift our fuel-based societies to electrified societies, with the great help of power electronic devices as well used in electricity generators as in electrical mobility [5]. This shift is generating huge challenges in terms of environmental footprint because it creates ecological impact transfers, mainly from fossil fuels to other resources depletions and electrical equipment manufacturing and end-of-life impacts [6].

Our eco-design study is based on a commercial solar power inverter. This widely manufactured product generally includes an important area of printed circuit board (PCB), which contributes significantly to the ecological impacts of the final product [8]. The PCB's contribution could become the largest one in a circular economy model were easy-to-dismantle parts like casing or inductors could be recovered at product's end-of-life. We selected two solar micro-inverters with and used their design as a candidate for our study. To sum-up, in terms of thermal design, both rely on a bottom side, through-PCB cooling. This choice enables the designers to exclusively use surface mounted (SMD) power MOSFET transistors, hence reducing the manufacturing cost. The applied design relies on a top-side cooling for the DC-DC stage, where the thermal study enables a wider spectrum of investigations. The design uses a more mainstream inverter architecture enabling more generally applicable rules.

II. Power Electronics Reference FR4 Design and Adaptations for PLA/Flax Substrate

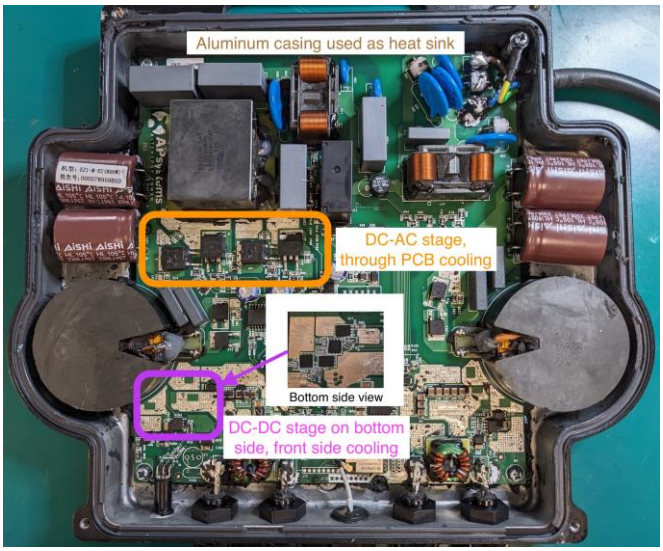

Fig. 1. APSystems inverter, PCBA in its casing, top side view

The demonstrators focus on the DC-AC stage, its associated control and electromagnetic compatibility (EMC) filters.

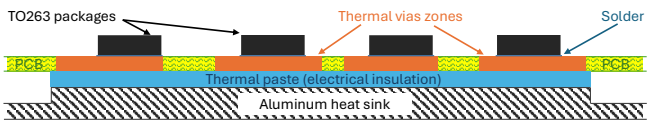

Fig. 2. Cross section view of DC-AC stage thermal dissipation

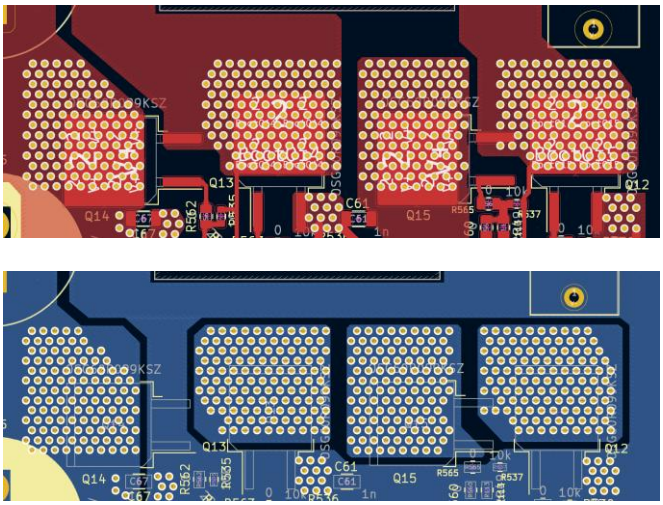

Fig. 4. PLA/flax adaptations: layers of the DC-AC MOSFET bridge

A. FR4 PCB reference design

A first step of the study involved the design of the DC-AC stage with routing of the 4 layers on a traditional FR4 PCB according to usual design aspects of such power-electronics functionality..

The reference PCB's thermal design (Fig. 3) has the following characteristics: 0.4mm diameter thermal vias with 1 mm pitch and an average number of 170 vias under each MOSFET (it varies slightly because of the layout constraints). The 1.55 mm commercial PCB has standard 35 µm copper layers, we therefore designed with vias made with standard 20 µm copper electroplating.

B. PLA/flax PCB, design adaptations

Previous works on the PLA/flax substrates showed some manufacturing constraints, leading to design

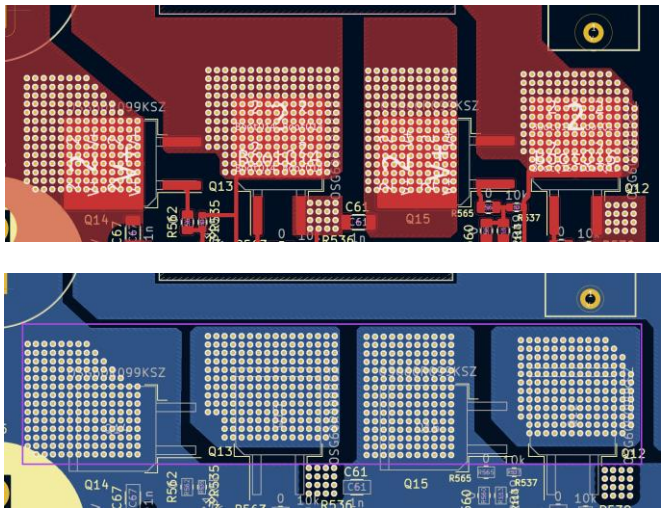

Fig. 3. Top (red) and bottom (blue) layers of the DC-AC MOSFET bridge with heat sink excange area in violet rectangle

adaptations [1]. For this particular design, the main constraints were the 2 copper layers limitation and minimum via diameter limited to 0.6 mm.

1) Thermal vias adaptations

Because of larger diameter, vias were spaced with a 1.4 mm pitch. The PLA/flax composite mechanical properties are below the usual parameters of FR4 (an aspect still under studies), we therefore had a

conservative approach, avoiding the weakening of the substrate by a too fine pitch. In order to provide a comparable amount of thermal conductor section (copper vias, see modeling in Chapter IV) we used an interlaced layout pattern in place of the original rectangular pattern (Fig. 4). This results in an average number of 118 vias per transistor. In the reference (recommended) design, vias are filled with solder, it contributes to enhance the thermal conductivity. In our design only the vias directly underneath the D2PAK (or TO-263) package thermal pad were filled. To calculate the filled section of vias in TABLE I. we counted the vias found underneath the component only.

TABLE I. THERMAL VIAS GEOMETRY

Design	For each transistor thermal pad				
	Via diameter	*Vias count*	*Filled vias*	*Copper section*	*Filler section*
Reference design	0.4mm	170	99	4.06mm^2	10.1mm^2
PLA/Flax design	0.6mm	118	56	4.30mm^2	13.8mm^2

The PLA/flax composite thermal diffusivity was characterized in [1], it is very close to that of pure PLA. We can therefore assume that the composite thermal conductivity is also very close to that of pure PLA (estimated between ~0.1-0.2 W.K^{-1}.m^{-1}). The lower glass transition temperature compared to epoxy-resin's one can imply to increase the conductivity of the thermal vias by design, in order to decrease the working temperature of the substrate at inverter's nominal power. To do so we need to raise the density of vias. We had a conservative approach in our design because of lack of knowledge on the mechanical limits of the PLA/flax composite. Thus, the present layout for these D2PAK packages is not optimal in terms of thermal resistance compared to state-of-the-art designs [7]. Further studies will allow us to reduce the performance gap. Still, with our design adaptations, the larger diameter combined with the pattern modification will lead to a smaller thermal resistance.

2) Design modifications related to the 2 layers limitation

The PLA/flax PCB is available with only 2 copper layers constrained the design, but it could also be a deliberate eco-design choice to limit the number of copper layers. Indeed, from a circular economy point of view, the eco-designer should limit the amount of copper present on the board to its strict functional

necessity (e.g. to control current density and parasitic inductances, and in general to meet EMC requirements).

In our case, regarding the thermal design, as visible on Fig. 4, the 2 layers limitation led to modifications of the bottom layer compared to the reference, with a slight decrease of 9.5% of the 12 cm^2 exchange area with the heat sink but the thermal resistance will not increase proportionally, because this area was not concerned with thermal vias. Maintaining the same area would have required a modification of the MOSFET implementation and of the heat sink milling. Another point is that the absence of the 2 internal copper layers also has thermal consequences but as it will be seen in Chapter IV, their contribution to reducing the thermal resistance is in the end might be negligible.

3) Design adaptations related to the substrate's mechanical properties

We set a smaller track width to 0.24 mm (10 mils) and added a teardrop shape to each track connection to a through-hole pad. The double via mindset on conductor tracks (practice of redundancy) was also systematically adapted to increase reliability.

C. Eco-demonstrators manufacturing

The reference design PCB was produced by a common PCB manufacturer on an FR4 1.55 mm standard 4 layers stackup. Vias are 20µm copper electroplated, and all copper layers are 35µm thick.

Still because of availability considerations, the eco-designed, sustainabledemonstrator was made on a substrate with nonstandard thickness (1.17mm). It was manufactured with standard subtractive processes and with copper electroplated (20µm) vias.

Because of thermal limitation properties of the bio-substrate, PCB's assembly was performed at reduced temperature, with tin-bismuth alloy (Sn42Bi57.6Ag0.4) solder paste (SMD parts) and solder wire (through-hole parts) with a 138 °C melting point temperature.

III. EXPERIMENTAL PART: THERMAL CHARACTERISATION

A. Post-assembly analysis

To ensure repeatability, a solder paste stencil should be used. But in our case the manual dispense of the solder paste, combined with the differences between the 2 kinds of paste led to inhomogeneous thermal via filling during the SMD soldering process. The thermal vias zones directly underneath the DPAK packages were therefore visually and X-Ray checked. TABLE II. describes these results for Q14 transistor because it is the one that is implemented with a contact-thermocouple during the thermal tests.

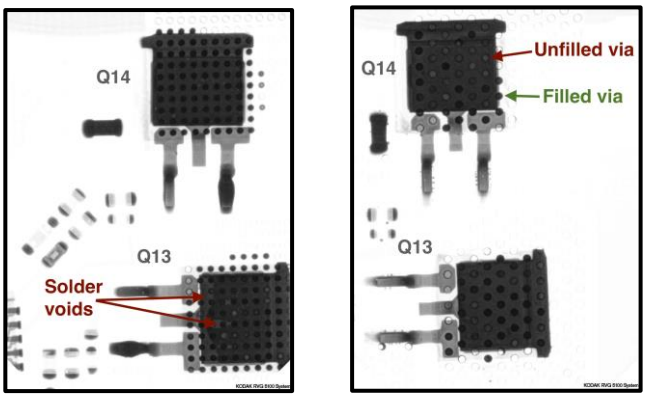

Fig. 5. Q14 / Q13 X-Ray views: FR4 design (left) and PLA/flax (right)

On the FR4 board, the X-Ray pictures show some significant solder voids underneath Q13 transistor, but thermal vias located below the drain pads are globally well filled, especially for Q14. This is not the case for the PLA/flax board, probably due to an insufficient deposit of solder paste, or the reduced via diameter, due to the more uneven wall (which is due to the natural fiber-reinforcements). On the other hand, the sustainable sample has almost no visible solder voids.

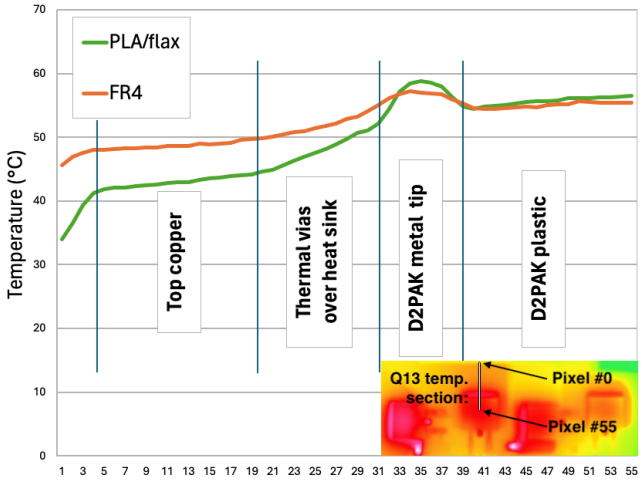

Fig. 9. Temperature profile on PCB and Q13 surface (working point #2)

TABLE II. Q14 MOSFET THERMAL VIAS CHARACTERISTICS

Design	*For Q14 transistor thermal pad*		
	Number of filled vias	*Individual via filled section*	*Resulting filled section*
Reference design	90	0.10mm^2	9.16mm^2
PLA/Flax design	21	0.25mm^2	5.17mm^2

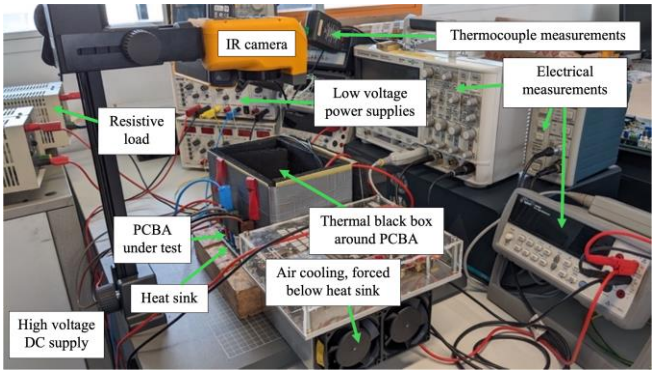

Fig. 7. Bench setup for thermal and electrical characterization

B. *Thermal characterisation setup*

1) DC-AC bridge control

On the referenceproduct, the DC-AC structure is driven by a sinus pulse width modulation (PWM) with variable switching frequency, from 150 to 350 kHz. On our demonstrators, to simplify, we apply a similar

command but in open loop at a fixed 167 kHz frequency. And the output is a resistive load instead of the power network.

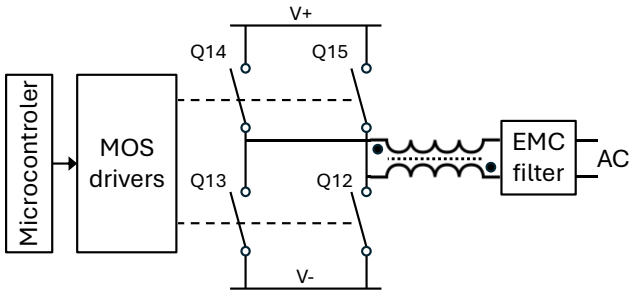

Fig. 6. DC-AC inverter bloc diagram

We took measurements for 3 working points, and input / output power measurements provide an indicative value of thermal losses; they are mainly located in the switching MOSFETs, but also a bit in the output coupled inductor.

TABLE III. ELECTRICAL WORKING POINTS

	DC voltage (V)	*Input power (W)*	*Output power (W)*	*Losses (W)*
Point #1	100	54.7	50.2	4.5
Point #2	100	181	167	14
Point #3	200	424	395	29

2) Thermal instrumentation

The main measurement is done with an infrared imaging camera. To ensure a homogeneous emissivity of the area of interest, it was coated in matt black following the procedure described in [11] and a black box was used to reduce the ambient light noise. A second measure is on the bottom side of the PCB, just underneath the Q14 drain pad, thanks to a thermocouple in sandwich between the PCB and the thermal paste. A third measurement is a thermocouple glued on the bottom side of the aluminum heat sink, underneath Q14. To reduce the thermal time constant, forced convection is used for cooling underneath the heat sink from right to left (Fig. 7).

C. Thermal characterisation results

Although the 4 transistors generate the same losses, the infrared imaging shows some small heterogeneities. On the images, only the bridge zone was black coated (MOSFETs and close SMD parts), temperature of further parts should be analyzed with caution.

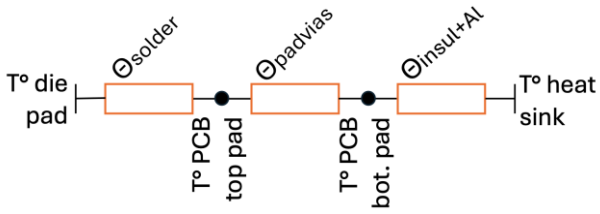

Fig. 10. Thermal diagram from transistor die pad to back of heat sink

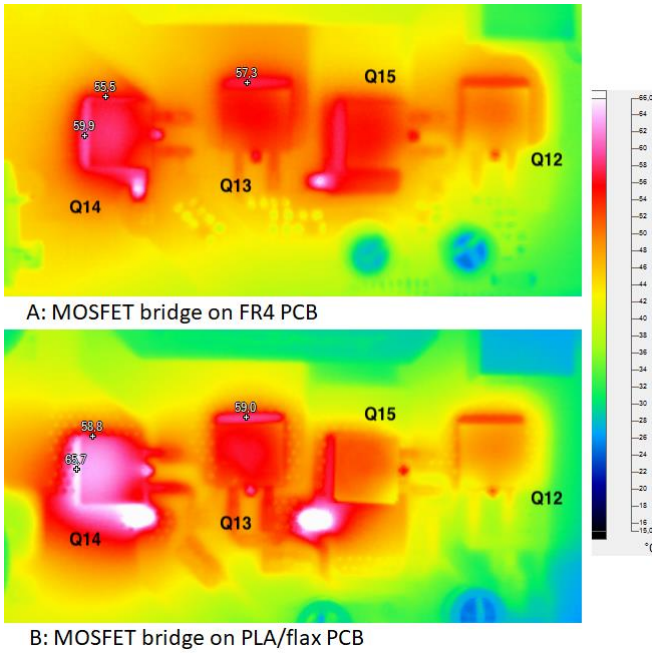

Fig. 8. Infrared imaging at the #2 working point (167W)

The infrared imaging shows a higher temperature on PLA/flax board parts compared to FR4 board. Heat is better sunk with FR4 design than with PLA/flax. Two markers are placed at the highest temperature points of Q14 / Q13 packages (die pad tip), and one on the PCB's surface, just over Q14.

For the 3 electrical working points (TABLE III. , temperatures on Q14 package's die tip are detailed in TABLE IV. with the temperatures of the underneath thermocouples.

TABLE IV. TEMPERATURE AT SELECTED WORKING POINTS (°C)

	FR4 Q14 die tip	PLA Q14 die tip	FR4 PCB top	PLA PCB top	FR4 PCB bottom	PLA PCB bottom	FR4 Heat sink	PLA Heat sink
# 1	31.5	35.5	30.5	33.5	26	27	24	25
# 2	60	66	55.5	59	42	38	36	31.5
# 3	105	135	98	105	64	60	48	42

First conclusions that can be drawn from these measurements are:

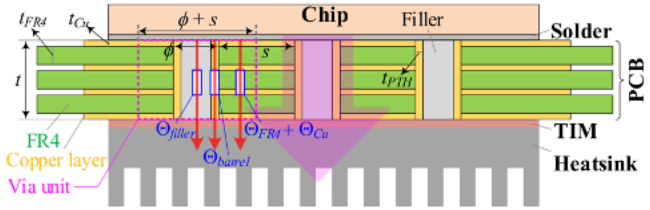

Fig. 11. Shen et al. thermal model of through-PCB heat transfer

- For all interfaces (Fig. 7), the temperature differences (ΔT) are always larger with the PLA/flax design except for the heat paste + heat sink one which are shared by both designs. The performance of the PLA/flax design does not reach the FR4 reference one.
- The higher thermal resistivity of the PLA/flax substrate compared to FR4 can also be observed on the surface of the PCB: temperature is decreasing faster all around the hot spots and surrounding parts are colder. The temperature profile from the inductor to the center of Q13 (Fig. 9) shows a faster decrease on PLA/flax PCB, although the package temperature is slightly higher.
- Finally, it is noticeable that the highest temperature on PCBs is in fact reached on the 2 ceramic capacitors (white spots on Fig. 8) decoupling the V+ supply. They are placed as close as possible to the bridge's upper transistors and therefore collects their heat; intense switching current flowing through capacitors with a not low enough equivalent series resistance (ESR) is probably the cause of this overheat.

IV. Discussion

A. *Analytical model of thermal vias*

To calculate our vias thermal equivalent resistance ($\Theta_{padvias}$, on Fig. 10), we used the thermal model elaborated by Shen et al. [12], which matches our design structure. It decomposes this thermal resistance into 3 parallel parts (Fig. 11): the via's copper barrel (Θ_{barrel}), the filler (Θ_{filler}, if applicable), and the substrate + copper layers ($\Theta_{FR4} + \Theta_{Cu}$, including internal copper layers if any). The latter depends on the pattern used for our vias layout (FR4 on Fig. 3 and PLA/flax on Fig. 4).

It is worth noting that our PLA/flax PCB is only 1.17 mm thick because of the experimental nature of it. To produce a fair comparison with FR4, we also computed the results for a standard 1.55 mm PCB thickness.

In our eco-design, the thermal vias area is larger than the D2PAK pad area. Vias that are not underneath the pad were not filled with solder paste. To properly calculate the contribution of these, one must consider the thermal gradient measured on Q13 pad (Fig. 9). To simplify, we chose to present a pessimistic thermal resistance result (solely the contribution of D2PAK pad underneath vias) and an optimistic one (all vias contribute as they were all placed underneath the pad, at its temperature).

TABLE V. EQUIVALENT PCB'S THERMAL RESISTANCE FOR ONE PAD

Thermal resistance (°C/W)	*For one thermal pad (filled vias underneath pad)*		
	FR4 PCB	*PLA/flax PCB*	*Std. 1.55mm PLA/flax PCB*
One filled via	95.6	57.0	75.5
One unfilled via	153.4	77.4	102.6
Pad vias (filled)	0.97	1.02	1.35
Surounding vias (unfilled)	2.16	1.25	1.66
Total (optimistic)	0.56	0.48	0.64
Total (pessimistic)	0.97	1.02	1.35

Because of their larger diameter, filled vias on 1.55 mm PLA/flax PCB should have a thermal resistance of 51.9 °C/W (half that of FR4 design), but the weaker result of 75.5 °C/W displayed in TABLE V. is due to the low-temperature solder paste poor conductivity: tin-bismuth alloy is only around 22 $W.K^{-1}.m^{-1}$ compared to about 50 to 60 $W.K^{1}.m^{1}$ for tin-lead or tin-copper SAC 405 standard solder paste. Shen & al.

showed in [12], that optimal diameter for thermal vias is 0.6 mm when filled with a 50 $W.K^{-1}.m^{-1}$ solder paste and only 0.35 mm at 25 $W.K^{-1}.m^{-1}$. In the future, this finding has to be included in our design constraints because it conflicts with the drill diameter low limit for our PLA/flax substrate; a tradeoff has to be found.

Another important conclusion derived from the analytic model is that the thermal conductivity of the substrate plays a minor role in the total value (a few percent), and that just using a slightly denser pattern of vias compensated the 2 times lower conductivity of PLA/flax.

Finally, as seen in TABLE II. Q14 vias underneath the pad were not properly filled. Considering the exact number of filled vias for each PCB, we computed the equivalent thermal resistance for Q14's pad in TABLE VI.

TABLE VI. EQUIVALENT PCB'S THERMAL RESISTANCE FOR Q14 PAD

Thermal resistance (°C/W)	*For Q14 thermal pad*	
	FR4 PCB	*PLA/flax 1.17mm PCB*
Pad & filled vias	1.06	2.71
Pad & surronding unfilled vias	1.80	0.82
Total (optimistic)	0.55	0.50
Total (pessimistic)	1.00	1.22

B. Experimental results analysis

These theoretical results match the experimental results: Q14's pad has a slightly higher equivalent resistance for the PLA/flax design, due to poor filling of vias. Results would be much worse with a standard 1.55 thickness, and this is mainly due to the poor conductivity of the filler paste.

1) Solder paste issue

The thermal resistance of the solder paste between the die pad and PCB pad is generally neglected in this kind of applications because of its small vertical dimension (thin layer). In our case it seems that the almost 3 to 1 solder paste conductivity ratio makes a difference: in TABLE IV. for the same thermal flux of working point #2, the ΔT between Q14 die tip and the PCB top pad jumps from 4.5°C (FR4 design) to 7°C (PLA-flax). No accurate calculation can be made from this because the PCB top pad temperature is picked on the IR imaging as close as possible to the package but is of course lower than the real value underneath the die pad.

2) Design enhancements

Based on the under-performing results of part III, we can propose some enhancements.

- Filled vias must be filled properly, i.e. using a stencil for solder paste deposit even for prototypes.
- Interlaced pattern is a good choice to increase vias density, but larger via diameter is not, especially without a high conductivity solder paste as filler.
- Work must be done to allow the drilling of small via diameters in the PLA/flax substrate.
- For both designs, the ΔT across the thermal paste used as an insulator between the PCB bottom and the aluminum heat sink is a bit high; a quick approximative calculation shows its thermal conductivity is about 2 $W.K^{-1}.m^{-1}$. It could be replaced with a better paste with 4 times higher conductivity.

3) Limitations of the experimental results analysis

We limited the theoretical work on analytical modeling. Finite element modeling-based simulation would provide additional information and accurate consideration of the thermal gradient around the die pad.

On both designs, a lower temperature is observed on the two transistors closer to the center of the board (Fig. 1 & Fig. 8). This is probably related to the direction of the air-cooling flow below the heat sink (Fig. 7), which creates a temperature gradient from right to left. Using an air flow perpendicular to the line of MOSFETs would be more appropriate, and could discard the possibility of the effect originated from the layout.

V. CONCLUSION

With this power electronics demonstrator, we successfully proved that a complex design heat transfer along the thickness of the PCB can be achieved on latest environmentally friendly bio-substrates. With some design adaptations, thermal vias structures can be efficiently implemented.

At this stage, we should keep in mind that the main issues are related to the temperature limitation during the assembly of the PCB which must be done below 200°C, at the risk of damaging the flax fibers. It implied the use of tin-bismuth low-temperature solder alloy which has limited thermal conductivity, when used as a via thermal filler. It is worth noting that other low-temperature indium alloy based seem to also have this poor thermal conductivity flaw (and is a more expensive commercial option).

We chose to use filled vias with larger diameter, but it is not a good practice from an eco-design point of view: it increases the used amount of tin and other metals which are more critical resources than copper. To propose a rule of thumb, reaching a low thermal resistance in a vias zone is mainly achieved through a good density of high conductivity metals in the vias zone volume. This is much better reached with copper than with other metals. Although it increases the drilling intensity at manufacturing, the best eco-design practice is probably to use very dense pattern of small unfilled vias. This is especially sensible when soldering is using low temperature alloys with limited thermal conductivity.

The temperature reached in the PCB is also related to the limited heat conduction through the insulating thermal paste between the PCB and the aluminum heat sink. Its thickness cannot be reduced because of the required electrical strength. Thus, enhancing the thermal vias design may not be enough. That would mean to abandon the through-PCB cooling to switch to top case cooling schemes. Because it increases complexity, it has consequences in terms of manufacturing cost and maybe in terms of product's ecological impacts.

T he reliability of the demonstrator should also be investigated. At full power, the temperature of the substrate is above its glass transition temperature. No warping is observed because the hot zone is laid on the heat sink through the thermal paste. But the mechanical ageing should be studied, notably at the substrate and copper interface.

ACKNOWLEDGMENTS

We acknowledge Meshlin company for providing the PLA/flax PCB substrates, as well as BME-ETT (and UniPCB Kft.) and UGA-CEDMS facilities for the PLA/flax PCB manufacturing and assembly.

REFERENCES

[1] Farkas, C., Gál, L., Csiszár, A., Grennerat, V., Jeannin, P. O., Xavier, P., ... & Géczy, A. (2024). Sustainable printed circuit board substrates based on flame-retarded PLA/flax composites to reduce environmental load of electronics: Quality, reliability, degradation and application tests. *Sustainable Materials and Technologies*, *40*, e00902.

[2] Nair, R. R., Wolansky, J., Uhlig, K., Solgi, A., Teuerle, L., Zhang, T., ... & Leo, K. (2024). Leaftronics: Natural lignocellulose scaffolds for sustainable electronics. *Science Advances*, *10*(45), eadq3276.

[3] Zhang, Z., Biswal, A. K., Nandi, A., Frost, K., Smith, J. A., Nguyen, B. H., ... & Iyer, V. (2024). Recyclable vitrimer-based printed circuit boards for sustainable electronics. *Nature Sustainability*, *7*(5), 616-627.

[4] V. Grennerat, P. Xavier, P. -O. Jeannin, N. Corrao and A. Géczy, "High-Speed Digital Electronics Board on a Novel Biobased and Biodegradable Substrate," *2023 46th International Spring Seminar on Electronics Technology (ISSE)*, Timisoara, Romania, 2023, pp. 1-5, doi: 10.1109/ISSE57496.2023.10168477.

[5] R. Singh, P. Paniyil and Z. Zhang, "Transformative Role of Power Electronics: In solving climate emergency," in *IEEE Power Electronics Magazine*, vol. 9, no. 2, pp. 39-47, June 2022, doi: 10.1109/MPEL.2022.3169317.

[6] J. Huber, L. Imperiali, D. Menzi, F. Musil and J. W. Kolar, "Energy Efficiency is Not Enough!," in *IEEE Power Electronics Magazine*, vol. 11, no. 1, pp. 18-31, March 2024, doi: 10.1109/MPEL.2024.3354013.

[7] D. S. Gautam, F. Musavi, D. Wager and M. Edington, "A comparison of thermal vias patterns used for thermal management in power converter," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, USA, 2013, pp. 2214-2218, doi: 10.1109/ECCE.2013.6646981.

[8] Musil, F., Harringer, C., Hiesmayr, A., & Schoenmayr, D. (2023, May). How life cycle analyses are influencing power electronics converter design. In *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management* (pp. 1-9). VDE.

[9] Géczy, A., Csiszár, A., Xavier, P., Corrao, N., Rauly, D., Kovács, R., ... & Gál, L. (2022, December). Thermal and RF characterization of novel PLA/Flax based biodegradable printed circuit boards. In *2022 IEEE 24th Electronics Packaging Technology Conference (EPTC)* (pp. 329-333). IEEE.

[10] Krammer, O., Hambuch, G., Bátorfi, R., Illés, B., & Géczy, A. (2024, October). Investigating the Copper Peel and Solder Joint Shear Strength on Biodegradable Substrates. In *2024 IEEE 30th International Symposium for Design and Technology in Electronic Packaging (SIITME)* (pp. 262-265). IEEE.

[11] L. Dupont, Y. Avenas and P. -O. Jeannin, "Comparison of Junction Temperature Evaluations in a Power IGBT Module Using an IR Camera and Three Thermosensitive Electrical Parameters," in *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1599-1608, July-Aug. 2013, doi: 10.1109/TIA.2013.2255852.

[12] Y. Shen, H. Wang, F. Blaabjerg, H. Zhao and T. Long, "Thermal Modeling and Design Optimization of PCB Vias and Pads," in *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 882-900, Jan. 2020, doi: 10.1109/TPEL.2019.2915029.