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A novel approach of single-device VO_2 oscillator for reconfigurable Boolean logic

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ABSTRACT

Vanadium dioxide (VO_2) exhibits a current-driven insulator–metal transition that gives rise to pronounced hysteresis and self-sustained relaxation oscillations under appropriate biasing, making it an attractive candidate for unconventional computing architectures. In this work, we demonstrate that a single triangular-channel VO_2 device can be reconfigured to perform multiple Boolean logic operations by encoding logic states in the presence or absence of oscillations, without modifying the device structure or adding auxiliary logic circuitry.

Using a dual-input current scheme, we first experimentally identify a well-defined oscillation window between 50 μA and 300 μA, within which the VO_2 channel operates in its negative differential resistance regime. Logic "1" is defined by sustained oscillations at the output, while logic "0" corresponds to a quiescent (non-oscillatory) state when the device is either insulating or fully metallic. By appropriately selecting bias conditions for the two inputs, we experimentally realize AND, OR, XOR, and NOT logic functions in a single VO_2 element. Additionally, these logic functions are validated through LTspice simulations using the same experimentally extracted threshold values. The triangular geometry of the VO_2 channel plays a key role in stabilizing the oscillation window by enabling spatially distributed Joule heating and gradual phase evolution, thereby improving operational robustness. Our results highlight a compact and bias-programmable approach to logic implementation in phase-transition materials, offering a pathway toward minimal-device-count logic elements and hybrid Boolean-oscillatory computing architectures based on VO_2.

Introduction

Vanadium dioxide (VO_2) is of particular interest among insulator–metal transition (IMT) materials because its resistivity and optical constants change abruptly near 68 °C [1,2]. The transition involves a structural change from a low-temperature monoclinic insulator to a high-temperature rutile metal [3] and can be triggered thermally [3–5], electrically [6,7], optically [8], or mechanically [9]. Substrate strain [10], film thickness [11], stoichiometry [7], and interfacial chemistry [12] shift the transition temperature and the magnitude of the resistivity jump, providing device designers with several parameters to adjust performance. These attributes have made VO_2 a leading candidate for neuromorphic elements, selector devices in crossbar memories [9], and relaxation oscillators [7] that emulate spiking neurons [1,13].

Materials that undergo an electrically driven IMT provide a compact pathway to computation because the same physical element can act as a switch, a memory, and under appropriate bias an autonomous oscillator [1]. Among these, VO_2 is especially attractive: its first-order IMT occurs near room temperature [14], it exhibits pronounced electrical hysteresis and Joule heating [3] and offers a direct and CMOS-compatible means of control [15,16]. Prior work has mainly exploited networks of VO_2 oscillators for phase-based computing and optimization tasks [1], where information is encoded in phase relationships or frequency locking across many coupled elements [5]. While such oscillator networks are powerful, they typically require auxiliary circuitry to generate oscillations, to set coupling strengths, and to read out phase complexity that can obscure the fundamental device-level computing primitives [17].

The devices based on VO_2 often exhibit current-controlled negative differential resistance (NDR) [18]. In the as-fabricated state, many amorphous or mixed-phase oxides are highly resistive and require a one-time electroforming step before a robust NDR response appears. Electroforming is achieved by applying a controlled current stress that

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nucleates a conductive filamentary path through the film. The process is governed by defect generation and ionic motion under the field, as well as by local Joule heating. Filament size, stability, and resistance are sensitive to the maximum forming current and the associated temperature rise; excessive stress can modify interfaces or crystallize amorphous regions, irreversibly altering later switching behaviour. After forming, VO_2-based channels typically switch because a portion of the path undergoes the IMT, consistent with the emergence of crystalline VO_2 within the filament [3,7,19–22].

The NDR characteristic in VO_2 devices appears in two broad forms. Many structures display a smooth S-type NDR, reflecting a heterogeneous transition and the gradual evolution of the temperature profile under current bias. Under certain conditions, devices exhibit a more abrupt snap-back, similar to that observed in NbO_x selectors; this mode can be useful from a functional perspective [19]. The proposed design of this study consists of a lateral two-terminal structure fabricated on a Si/SiO_2 substrate. A thin VO_2 film is patterned into a triangular channel geometry, with platinum (Pt) electrodes contacting the two ends of the triangle, a wide base and a narrow apex. This triangular geometry of the electrodes creates a non-uniform current density distribution along the channel length: the current crowds near the apex, where the local power density is highest (joule heating starts there). As a result, the insulator-to-metal transition nucleates at the apex and propagates toward the base under increasing bias, producing the abrupt snap-back NDR behaviour. A cross-sectional schematic and EDS elemental maps confirming the spatial distribution of vanadium, oxygen (the source of oxygen is from VO_2 and SiO_2), and platinum are shown in Fig. 1. In NDR cases, strong electro-thermal feedback couples the instantaneous current to local temperature, producing the hallmark hysteresis and enabling relaxation oscillations when the bias is placed within a finite current window, as shown in Fig. 2. Outside that window, the device is either fully insulating at low current or clamped metallic at high current, yielding a quiescent output behaviour that is directly exploitable for computational elements.

VO_2 provides a uniquely practical platform for reconfigurable computation because it combines a sharp, near-room-temperature IMT; strong, controllable NDR with hysteresis, and compatibility with simple two-terminal layouts. Electroforming establishes a conductive path in which the IMT can be driven repeatably, while electro-thermal feedback defines a stable oscillation window bounded by lower and upper current thresholds. When the operating point is within this window, the device

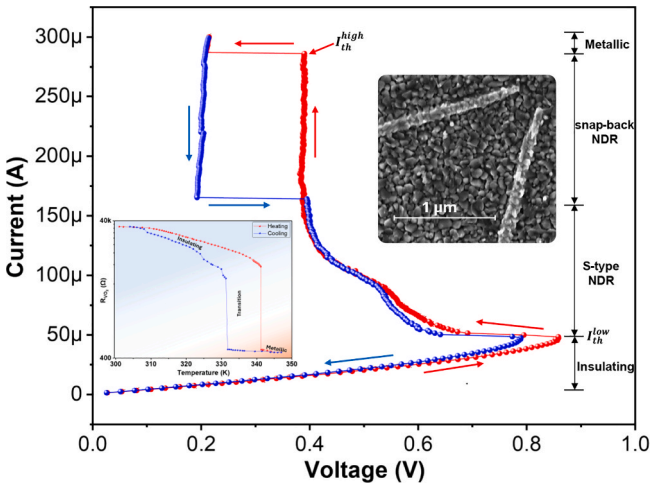

Fig. 2. Characteristics of the triangular VO_2 channel. IV characteristics of the VO_2-based triangular channel reveal a smooth S-type behaviour, accompanied by a notable phenomenon known as snap-back NDR. The inset images illustrate the R-T curve, prominently showing the transient response at 68 °C, along with the SEM image that shows the material's grain size.

behaves as a self-sustaining oscillator; when it is outside this window, it is quiescent [5]. These properties enable a single VO_2 resistor to realize multiple Boolean functions solely through bias programming, a device-level primitive that complements larger oscillator network approaches and motivates physically grounded, thermally aware compact models for circuit simulation.

Here, we take a complementary approach and ask a simpler question: what computation can a single VO_2 element perform on its own when driven by two programmable current inputs and observed at a single node? We show that the intrinsic electro-thermal dynamics of a single VO_2 resistor are sufficient to implement three Boolean gates: AND, OR, XOR, and NOT within one reconfigurable cell. The key is an oscillation-presence encoding: when the net device current lies inside a finite window bounded by a lower and an upper threshold (I_{th}^{low} and I_{th}^{high}), the device repeatedly traverses the insulator–metal transition IMT into metal- insulator transition MIT hysteresis and the output exhibits self-sustained relaxation oscillations (logic "1"); outside this window, the

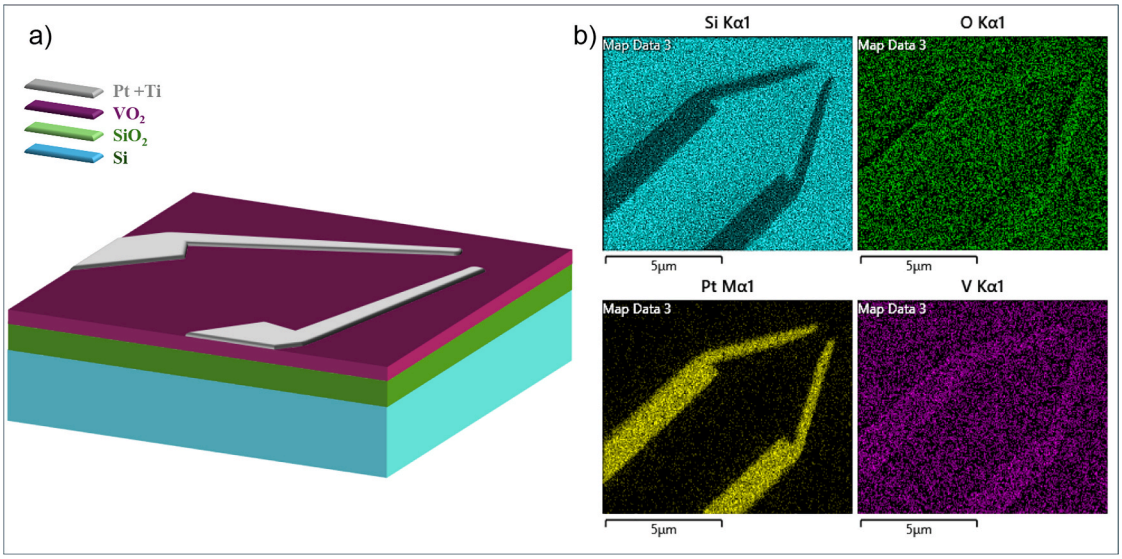

Fig. 1. Triangular VO_2 channel. (a) 3D cross-sectional schematic of the proposed lateral-triangular VO_2 device with Pt electrodes on Si/SiO_2 substrate. (b) Scanning electron microscope (SEM) with energy-dispersive X-ray spectroscopy (EDS) maps obtained from the highlighted region confirm the spatial distribution of the VO_2 components and the contact metallization; the false-color channels correspond to the element labels in each map.

output is quiescent because the device is either fully insulating or clamped metallic (logic "0"). With experimentally extracted thresholds fixed at $\mathbf{50\ \mu A \leq I_{VO_2} \leq 300\ \mu A}$ at 25 °C, proper biasing of the two inputs places each truth-table corner inside or outside the oscillation window, thereby realizing a desired gate without changing the device or adding active logic transistors.

In this work, we (i) fabricate and electrically characterize VO_2 device, (ii) extract I_{th}^{low} and I_{th}^{high} from IV characteristic, (iii) demonstrate AND, OR, XOR, and NOT experimentally using two independently programmable sources (I_A and I_B) as shown in Fig. 3, and (iv) confirm AND, OR, XOR, and NOT by circuit-level simulation with the same thresholds and device parameters.

Results

Triangle-drive characterization of the VO_2 channel

The triangular VO_2 channel was first examined under a single-source drive. The Keithley source meter, used as an input (I_B), was disabled, and a triangular waveform from the function generator was applied to the voltage-to-current converter (VCC). With the converter transresistance set by $R_2 = 50$ kΩ, the input current (I_A) was proportional to the generator voltage ($I_A = \frac{V_{in}}{R_2}$). The drive frequency was 100 Hz; the peak voltage stepped from 2 V to 6 V to sweep the current across the device's operating range. As shown in Fig. 4 (a-d), the output node V_{out} remains quiescent at low current and then develops self-sustained oscillations once the branch current reaches approximately 50 μA, marking the onset of the oscillation window. Increasing the peak of the triangular drive extends the portion of the cycle spent within this window, yielding longer oscillatory segments and a higher instantaneous oscillation frequency, consistent with current-controlled NDR behaviour. At the beginning of the oscillation window, the VO_2 channel oscillated at about 30 kHz. As the current increased along the channel response, the oscillation frequency rose continuously and reached approximately 200 kHz near 300 μA.

Fig. 4a shows the response of the VO_2 channel when the input V_{in} is 2 V corresponding to an input current [$I_A = \frac{V_{in}}{R_2} = 40\,\mu A$]. At this current level, the device is not driven into the NDR region and therefore remains in the insulating phase, with R_{vo2} approximately equal to 40 kΩ. Under this condition, the VCC which operates as a non-inverting amplifier, giving an output voltage close to $2V_{in}$, as described by Eq. (1).

$$\boldsymbol{V_{out} = \left[1 + \frac{R_{VO_2}}{R_2}\right] V_{in}} \tag{1}$$

Fig. 4b illustrates the onset of oscillatory behavior as the VO_2 channel enters the negative differential resistance (NDR) region. As the current reaches the threshold, oscillations begin to appear near the peak of the triangular input. During the decreasing slope of the input signal, the oscillations persist even when the current drops below the lower threshold (~50 μA), which is attributed to the hysteresis behavior of the VO_2 phase transition.

In this regime, the VO_2 resistance dynamically oscillates between approximately 1 kΩ and 20 kΩ, corresponding to repeated transitions between the metallic and insulating states. This oscillatory behavior remains stable and extends over a wider current range as the input current is further increased, up to approximately 120 μA, as shown in Fig. 4c and d.

Square-wave operation and oscillation window

With the oscillation window approximately at 50–300 μA, the large window is due to the triangular VO_2 channel [19], as shown in Fig. 2. A square wave was used to drive to map each truth-table corner to an output state and to quantify operating margins. When the net device current $I_{VO2} = I_A + I_B$ was below 50 μA the channel remained insulating and V_{out} was quiescent; when I_{VO2} was above 300 μA the device clamped metallic and oscillations quenched. Sustained relaxation oscillations (logic "1″) appeared only when I_{VO2} lay strictly within the window. Close to the boundaries we observed the expected degradations: near 50 μA, the oscillation onset was intermittent while near 300 μA the frequency decreased and the waveform collapsed abruptly as the metallic phase stabilized. Representative output traces in Fig. 5, together with the corresponding truth table, show flat segments for logic '0' and periodic spike trains for logic '1'. The oscillation frequency is approximately 30

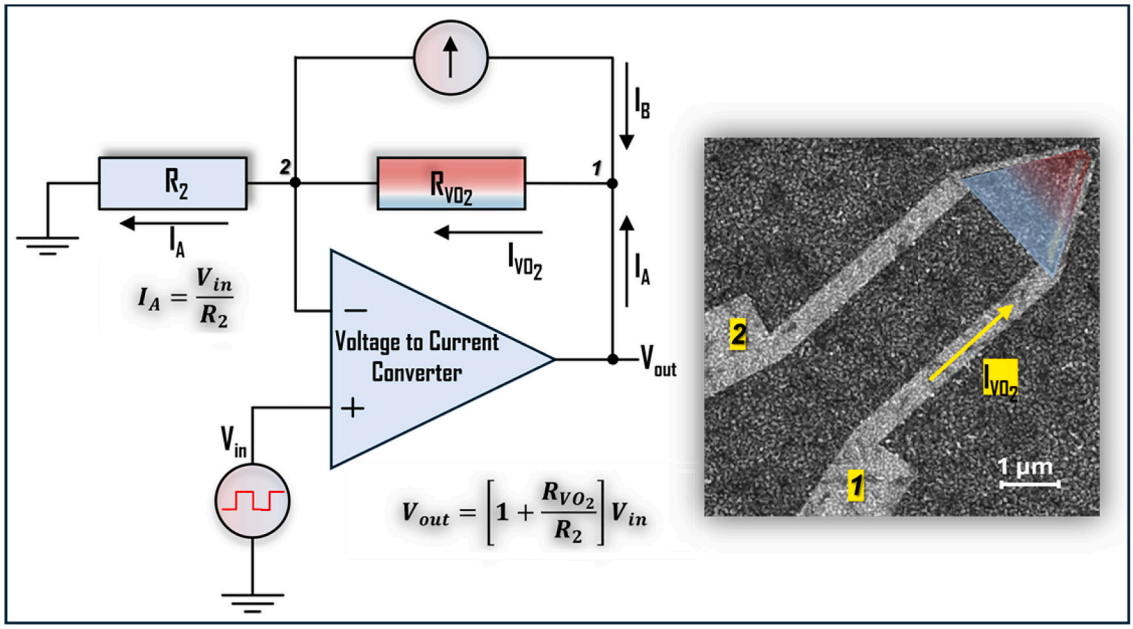

Fig. 3. Device concept, experimental configuration, and VO_2 channel morphology. Schematic of the experimental setup (showing the voltage-to-current converter based on an operational amplifier "I_A", the Keithley source meter used as a DC current input "I_B"), in which two controlled input currents, I_A and I_B, are algebraically combined at the output node (node 1), resulting in a net VO_2 branch current $I_{VO2} = I_A + I_B$. The inset SEM image shows the lateral triangular VO_2 channel used in this study, highlighting nodes 1 and 2, the active conduction region, and the direction of I_{VO2}.

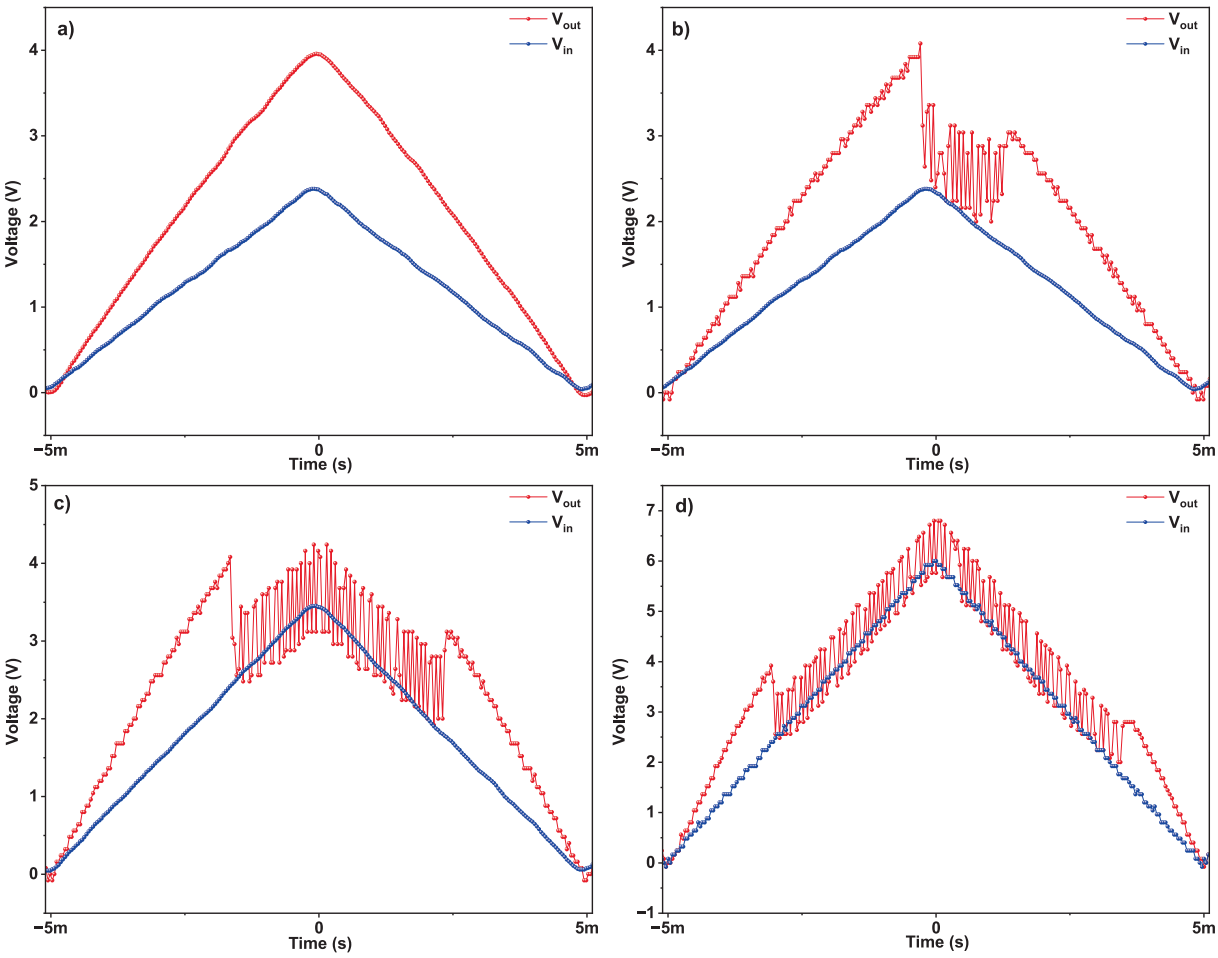

Fig. 4. Triangle-driven identification of the VO_2 oscillation window. a) A triangular input with a peak amplitude of ~2 V (corresponding to $I_A \approx 40$ μA) produces a smooth, non-oscillatory output, indicating that the VO_2 channel remains in the insulating phase with a resistance of approximately 40 kΩ. b) Increasing the peak input to ~2.5 V ($I_A \approx 50$ μA) initiates the onset of oscillations near the apex of the triangular waveform. At this point, the VO_2 resistance abruptly drops to ~1 kΩ, marking entry into the negative differential resistance (NDR) region. As the drive current decreases on the falling edge of the triangle and drops below the lower threshold, the device returns to the insulating state and oscillations cease. c and d) Further increasing the peak input voltage to 3, then to 6 V ($I_A \approx 60$ to 120 μA), broadens the temporal window over which oscillations are sustained, confirming stable operation within the NDR regime during both the rising and falling portions of the waveform.

kHz at the onset of the oscillation window (~50 μA) and increases progressively as the current rises, reaching a maximum of about 200 kHz near the upper limit of the window. As the current approaches and exceeds ~300 μA, the oscillations collapse abruptly, indicating the transition of the VO_2 channel into the fully metallic phase. This behaviour is consistent with current-controlled negative differential resistance (NDR) dynamics governed by electro-thermal feedback. These margins were used to program the single VO_2 cell to realize AND, OR, XOR, and NOT by selecting (I_A, I_B) pairs that place each input combination unambiguously inside or outside the oscillation window. In this experiment, we implemented four fundamental logic gates: AND, OR, XOR, and NOT and these gates were simulated using LTspice for analysis and verification purposes.

AND, OR, XOR, and NOT with a single VO_2 cell (square-wave drive)

We programmed the device by holding a DC "controller" current I_B and toggling input I_A with a square wave. Logic is encoded by oscillation presence at V_{out} (oscillation = 1, flat = 0), and the oscillation window is 50–300 μA.

AND: To implement an AND function, a small DC bias is applied, and the I_A square is used to introduce current. With an I_B of 10 μA and toggling between 0 and 40 μA, the four key points are as follows: (0,0) yields 0 μA (insulating, 0); (0,1) gives 40 μA (insulating, 0); (1,0) also results in 40 μA (insulating, 0); and (1,1) produces 50 μA (oscillating, 1). This behavior aligns with the expected outcome of the AND function, as illustrated in Fig. 5a.

OR: Setting a DC bias on I_B and using the I_A square to add current realizes OR. With $I_B = 50$ μA and I_A toggling between 0 and 60 μA, the four corners are: (0,0) → 0 μA (insulating, 0); (0,1) → 60 μA (oscillating, 1); (1,0) → 50 μA (right at the lower threshold with oscillating, 1); (1,1) → 110 μA (oscillating, 1). The behaviour matches OR as shown in Fig. 5b.

XOR: The XOR was emulated by biasing I_B high and pulsing I_A so that exactly one high should land inside the window while the other two corners land outside. With $I_B = 300$ μA, and $I_A = 0$ or 60 μA, both the high corners are metallic (≈360 μA), and both the low corners are insulating (0 μA), (0,1) → 300 μA (oscillating, 1); (1,0) → 60 μA (oscillating, 1) as shown in Fig. 5c.

NOT: With I_B set near the top of the window, the I_A pulse either keeps the device inside the window (low A) or pushes it above it (high A), inverting the input. In this experiment with $I_B = 300$ μA, the low state of $I_A = 0$ places I_{VO2} at the upper boundary (oscillating, 1). At this point, oscillations are marginal or quenched, and any additional current drives the channel into a metallic state, as shown in Fig. 5c when I_B is always high.

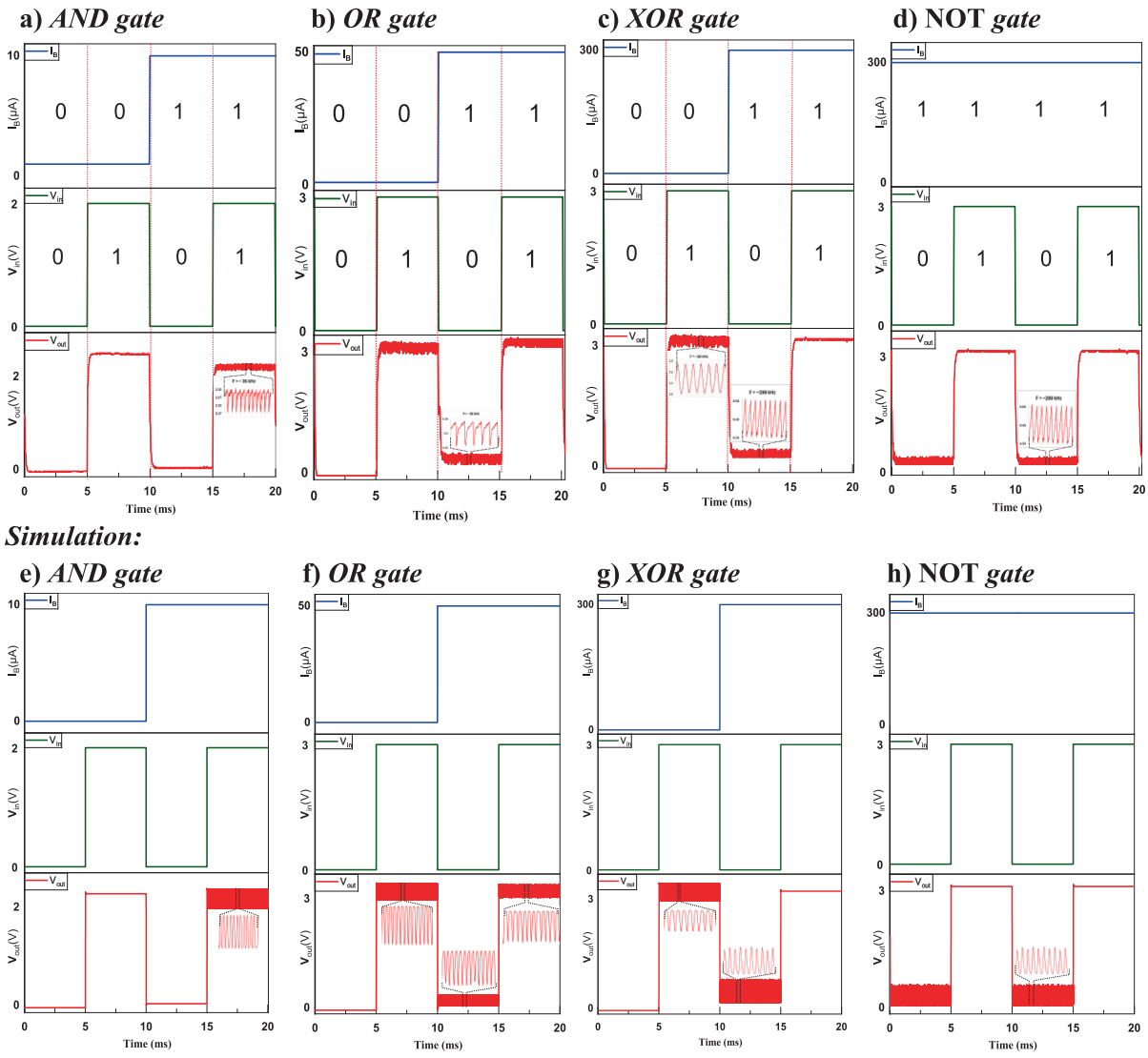

Fig. 5. Experimental and simulated realization of AND, OR and XOR logic gates using a single VO_2 oscillator.

LTspice simulation of reconfigurable VO_2 logic (single-cell, square-wave drive)

To validate the experimental observations, the VO_2 device was implemented in LTspice using a physics-based electro-thermal model that captures the current-driven insulator–metal transition (IMT) and the associated negative differential resistance (NDR). The simulation employed the same electrical circuit configuration shown in Fig. 3, ensuring direct consistency between experimental and numerical analysis. The VO_2 device was modelled using a lumped electro-thermal framework, where the temperature-dependent resistance is dynamically coupled to a thermal RC network based on the Cauer topology, enabling accurate representation of Joule heating and heat dissipation processes.

The thermal network parameters were adjusted according to the operating conditions of each logic function to reproduce the corresponding switching and oscillatory behaviour. This approach allows the model to capture the hysteresis and phase-transition dynamics of VO_2, as well as the oscillation window observed experimentally. Figs. 5(e–h) present the LTspice simulation results demonstrating the reconfigurable logic operation, including AND, OR, XOR, and NOT gates, achieved using the same VO_2 cell under different biasing conditions.

Experiment

Each graph has three panels: the top panel shows the bias current I_B supplied by a Keithley source, the middle panel shows the input voltage V_n converted to current I_A by using VCC via a 50 kΩ resistor [$I_A = \frac{V_{in}}{50k\Omega}$], and the bottom panel shows the output voltage V_{out}. Oscillatory output corresponds to logic "1", while a flat output corresponds to logic "0". Logic behaviour emerges when the current flows through VO_2 [$I_{VO2} = I_A + I_B$] falls within the oscillation window between I_{th}^{low} and I_{th}^{high}. a and e) AND gate, oscillations appear only when the combined current $I_A + I_B$ lies within the oscillation window. b and f) OR gate, oscillations occur when either I_A, I_B, or their sum $I_A + I_B$ falls within the oscillation window, resulting in three oscillatory cases. c and g) XOR gate, oscillations occur when either I_A or I_B individually lies within the oscillation window, while the combined current $I_A + I_B$ exceeds the upper threshold I_{th}^{high}, driving the device into the metallic state and suppressing oscillations. d and h) NOT gate: oscillations occur when $I_A = 0$, while the device is biased by I_B near the upper threshold I_{th}^{high}, placing the total current within the oscillation window (logic "1"). When I_A is applied, the combined current $I_A + I_B$ exceeds I_{th}^{high}, driving the VO_2 device into the metallic state and suppressing oscillations (logic "0"), thereby realizing the inversion operation.

Discussion

Our results show that a single triangular-channel VO_2 resistor can be programmed simply by biasing currents to implement a full set of basic Boolean operations. The key is the device's built-in electro-thermal feedback, which creates a well-defined self-oscillation window: when the net current through the VO_2 branch falls between 50 and 300 μA, the output exhibits relaxation oscillations (we interpret this as logic "1″); outside this range, the output becomes flat because the channel is either still insulating or fully driven into the metallic state (logic "0"). Using two independently controlled inputs that combine at the VO_2 branch (node 1), we chose bias points so that each truth-table corner lands either inside or outside the oscillation window. With this approach, we experimentally demonstrated AND, OR, XOR, and NOT, and reproduced these gates in LTspice using the same threshold values. In practice, the most stable operation occurs when the bias sits comfortably inside the window (about 60–290 μA). Near the boundaries, the behaviour becomes sensitive: oscillations can start intermittently close to 50 μA, while approaching and exceeding 300 μA leads to a reduction in oscillation frequency followed by abrupt quenching. These observations emphasise the need to maintain adequate noise margins when selecting operating points. However, the IV curve is sensitive to environmental temperature [23]; our sample was measured at 25 °C and 30 °C. An increase in temperature results in a decrease in the threshold voltage (V_{th}). Although the 5 °C temperature difference may seem minor, it corresponds to a V_{th} of approximately 0.85 V. Additionally, the low- and high-level values decreased by nearly 32%, narrowing the operating range as shown in Fig. 6. This study focused on the premise that two current inputs drive the VO_2 device; therefore, experiments were conducted at 25 °C. Future objectives include controlling the low and high levels at various temperatures to better define the input current margin and optimizing the geometry of the triangular channel.

This bias-programmable strategy is useful in several ways. First, it compresses logic functionality into a single two-terminal device, avoiding extra coupling networks or dedicated thresholding transistors and reducing interconnect overhead. Second, the oscillatory "1" naturally carries analogue information (such as frequency and envelope), which could be exploited for multi-level signalling or confidence-weighted decisions without changing the hardware. Third, because the same oscillation window governs four gates, the design rules are consistent and directly tied to the physical parameters of the triangular VO_2 channel (e.g., geometry, thermal impedance, and film quality). The close agreement between the measured and simulated gates indicates that compact, thermally informed models are sufficient for circuit exploration and provide a practical route toward scaling, variability studies, and reliability analysis.

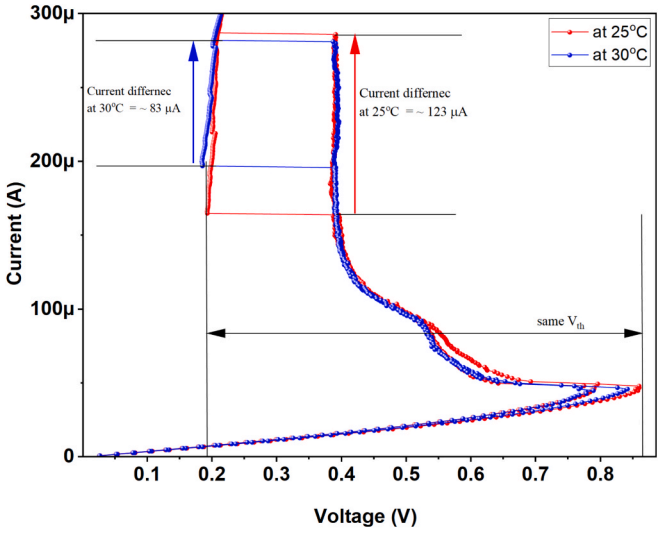

Fig. 6. Shows the IV curves vs. Temperature of the triangular sample, indicating that the IV curves are sensitive to environmental temperature.

Novelty and distinction from prior VO_2 logic

Previous VO_2-based logic demonstrations have predominantly relied on networks of coupled oscillators, multi-device configurations, or explicit thresholding and coupling circuitry, where logic states are encoded in phase relations, frequency locking, or collective dynamics [5,23–26]. In contrast, the present work demonstrates that a single VO_2 device, engineered with a triangular lateral channel, can function as a fully reconfigurable logic element by exploiting its intrinsic electro-thermal feedback and current-controlled oscillation window. Here, Boolean states are encoded solely in the presence or absence of self-sustained oscillations, without requiring device replication, external coupling networks, or phase readout circuitry. By bias programming two additive input currents, we experimentally realize AND, OR, XOR, and NOT operations within one physical VO_2 resistor and validation was performed using Ltspice to verify the behaviour of these gates based on the data extracted experimentally thresholds. This single-device, oscillation-based logic paradigm represents a shift from network-level computation toward device-level computational primitives, reducing circuit complexity while preserving the rich dynamics of phase-transition materials. The use of a triangular VO_2 channel further distinguishes this work by enabling a stable and extended oscillation window through spatially distributed Joule heating, providing a geometry-driven route to robust and scalable logic-in-matter.

Method

VO_2 fabrication and device geometry

Silicon substrates with a 300 nm thermally grown SiO_2 layer were used throughout. Prior to any deposition or patterning step, substrates were cleaned by oxygen plasma treatment to remove organic surface contamination and ensure uniform adhesion of the subsequent resist and metal layers. The 150 nm polycrystalline VO_2 functional layer was deposited over the SiO_2 layer by reactive RF sputtering from a metallic vanadium target. The deposition was carried out in a mixed Ar/O2 atmosphere at a chamber pressure of 1 mTorr with an Ar/O_2 flow ratio of 8:2, at a substrate temperature of 650 °C sustained for one hour. These conditions were optimised to produce near-stoichiometric polycrystalline VO_2 exhibiting a sharp and reproducible insulator-to-metal transition near 67–68 °C.

To connect the nanoscale EBL-defined electrodes with their connection pads to be more reliable for the four-probe station contact. Therefore, the eight lateral draft patterns that form the four triangular VO_2 channels were first fabricated. A photolithography process using positive photoresist was performed. The first part of all lateral electrodes started with 5 μm wide and extended two times to connect the pads squares (150x150 μm). The lateral electrodes metal stack, consisting of a 5 nm Ti adhesion layer followed by 25 nm Pt, was deposited by physical vapor deposition (PVD) using the AJA ATC system. The Ti layer ensures adhesion between the Pt and the VO_2 surface, while the Pt layer provides a chemically inert, thermally stable and low electrical resistivity contact. Lift-off process was performed after deposition to define the final electrode pattern. The nanoscale part of the electrodes for the triangular channels was patterned directly on the VO_2 surface using the Raith 150 electron-beam lithography system with PMMA 600 k as the e-beam resist at a spin speed of 4000 rpm. This part of the electrodes was designed to overlap with the draft electrodes (previous step) by 5 μm to ensure reliable electrical continuity, as shown in Fig. 7 as an example of one width. Following exposure and development, the bottom electrode patterns were ready for metal deposition. The EBL electrodes are deposited with the same previous procedure.

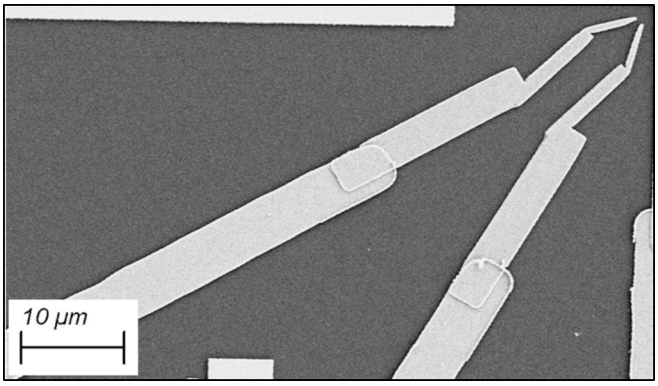

Fig. 7. One lateral triangular VO_2 channel, as an example of the four channels, outlines the two defined parts of the electrode fabrication steps.

Circuit connection and measurement workflow

The VO_2 device is driven by a voltage-to-current converter (VCC) built around a TL074 op-amp (non-inverting configuration). A function generator provides the input voltage V_{in} to the op-amp's + terminal. The op-amp output node V_{out} is connected to one terminal of the VO_2 channel; the return terminal of the device is tied to the VCC summing node through a series resistor R_2, which sets the transresistance. Thus, the drive current contributed by (input A) is $I_A = \frac{V_{in}}{R_2}$.

The op-amp is powered from symmetric rails (±15 V) to accommodate the transient swing required by the oscillatory regime. The VCC stability condition requires that the op-amp output voltage, $V_{out} = 1 + \frac{R_{VO2}}{R_2})*V_{in}$ remains below the supply rail throughout the entire oscillation cycle. With $R_2 = 50$ kΩ and ± 15 V rails, this is satisfied for $R_{VO2} < (\frac{V_{rail}}{V_{in}} - 1)*R_2$. Since the IV characterization (Fig. 2) confirms that R_{VO2} remains between approximately 1 kΩ and 40 kΩ across all operating conditions, the op-amp output stays well within its linear region at all programmed bias points. The IV characteristic is therefore an essential prerequisite for VCC design: it defines the R_{VO2} range against which R_2 and the supply voltage must be selected. For a device with a higher insulating-state resistance, R_2 would need to be reduced or the supply voltage increased to maintain current regulation stability.

A Keithley 2450 SourceMeter supplies the second, independent input I_B as a DC current (input B); its polarity is selected so that I_B either adds to or subtracts from I_A at the VO_2 node. In this experiment, four logic gates (AND, OR, XOR and NOT) were used to add direction. The oscilloscope (Agilent DSO1024A) monitors both V_{in} (generator reference) and V_{out} (node 1). A digital multimeter (Agilent 34401A) is placed in series to verify the branch current during calibration. The on-wafer probe station (Signatone probe station model S926) contacts the VO_2 pads; all instrument grounds share a single reference point to avoid ground loops. With this wiring, the net VO_2 current is the signed sum $I_{VO2} = I_A + I_B$, which determines whether the device is below threshold (insulating, no oscillation), within the oscillation window (logic "1"), or above the upper threshold (metallic, quenched).

CRediT authorship contribution statement

Salam A.W. Al-Abassi: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Software, Validation, Visualization, Writing – original draft. **Péter Neumann:** Writing – review & editing, Supervision, Resources, Project administration.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Peter Neumann reports financial support was provided by European Union through the HCHiP. Peter Neumann reports financial support was provided by National Research, Development and Innovation Fund of Hungary. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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Further reading

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